SECOND YEAR
FINAL REPORT
FOR
RESEARCH AND DEVELOPMENT STUDY
ON
DC TO DC CONVERTER
ENGINEERED MAGNETICS MODEL EMCR131A
CONTRACT NO. NAS5-10219
REPORT NO. 2071

PREPARED FOR
NATIONAL AERONAUTICS SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

Gulton Industries, Inc.

ENGINEERED MAGNETICS DIVISION • 13041 CERISE AVE., HAWTHORNE, CALIF.

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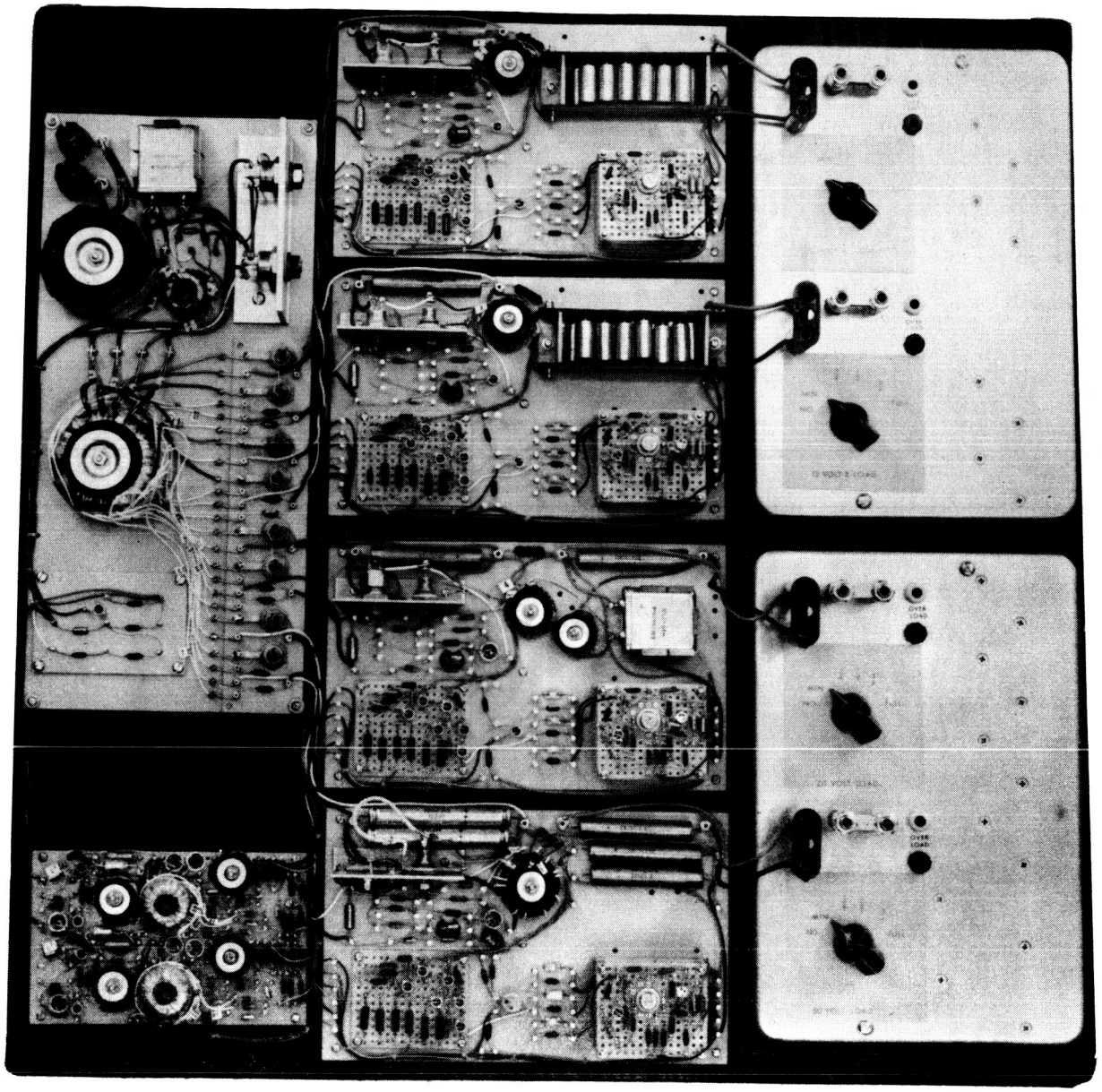

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SUMMARY

A. This summary covers the work performed on a research and development study program under NASA Contract NAS5-10219. The purpose of this study is to optimize the design of the existing Engineered Magnetics Model EMCR131 DC/DC Converter and thereby attain an improved version to be designated Model EMCR131A.

B. A block diagram of the basic approach to the Model EMCR131A design is shown in Figure 1. A square-wave current driven oscillator drives a toroidal transformer which has four isolated power outputs. These outputs vary in proportion to the input voltage but are so designed that they always exceed the required output voltage by at least 2 volts. Final regulation of each output is accomplished by separate free running switching-mode regulators which operate by chopping the input voltage and then filtering the resulting rectangular wave.

C. During the first quarterly period of effort, the overall approach of the EMCR131 was examined and confirmed. To make optimization possible, the free running switching-mode regulator circuit was analyzed in detail and an equation was obtained for output ripple in terms of the circuit parameters. This analysis revealed the importance of several circuit imperfections including resistance of a capacitor, switching times of a transistor, and hysteresis of a comparator. The effect of this capacitor resistance on the regulator design was evaluated with these effects in mind.

D. During the second quarterly period of effort, a twelve-volt free running switching-mode regulator was constructed using a low level circuit having a very small, controllable, hysteresis and short delay times. The regulator was then used to quantitatively check the analysis which was performed during the first quarterly period of effort. In order to evaluate the $R_C C$ durations of various capacitors, a triangle

current generator was constructed, and measurements were then made from an oscilloscope screen. Various forms of current limiting were investigated (in an attempt to improve the EMCR131 design), and various reliability techniques (parallel power stages, best two-out-of-three low-level networks, etc.) were considered.

E. During the third quarterly period of effort, a 50V free running switching-mode regulator was constructed using redundant low level circuits and redundant current limiting. Performance was tested and verified, including transfer functions of the low level majority circuit. An auxilliary power supply for the low level modules was designed and partially tested. The fusing of capacitors as a reliability measure was considered.

F. In the final period of effort, the design, construction and testing of the EMCR131A DC/DC Converter was completed. Nearly all design goals were met or exceeded. Reliability calculations indicate more than 90% probability of completing a 3 1/2 year mission with no failures and negligible drift. This report is a complete summary of all four periods of effort from basic assumptions through final design.

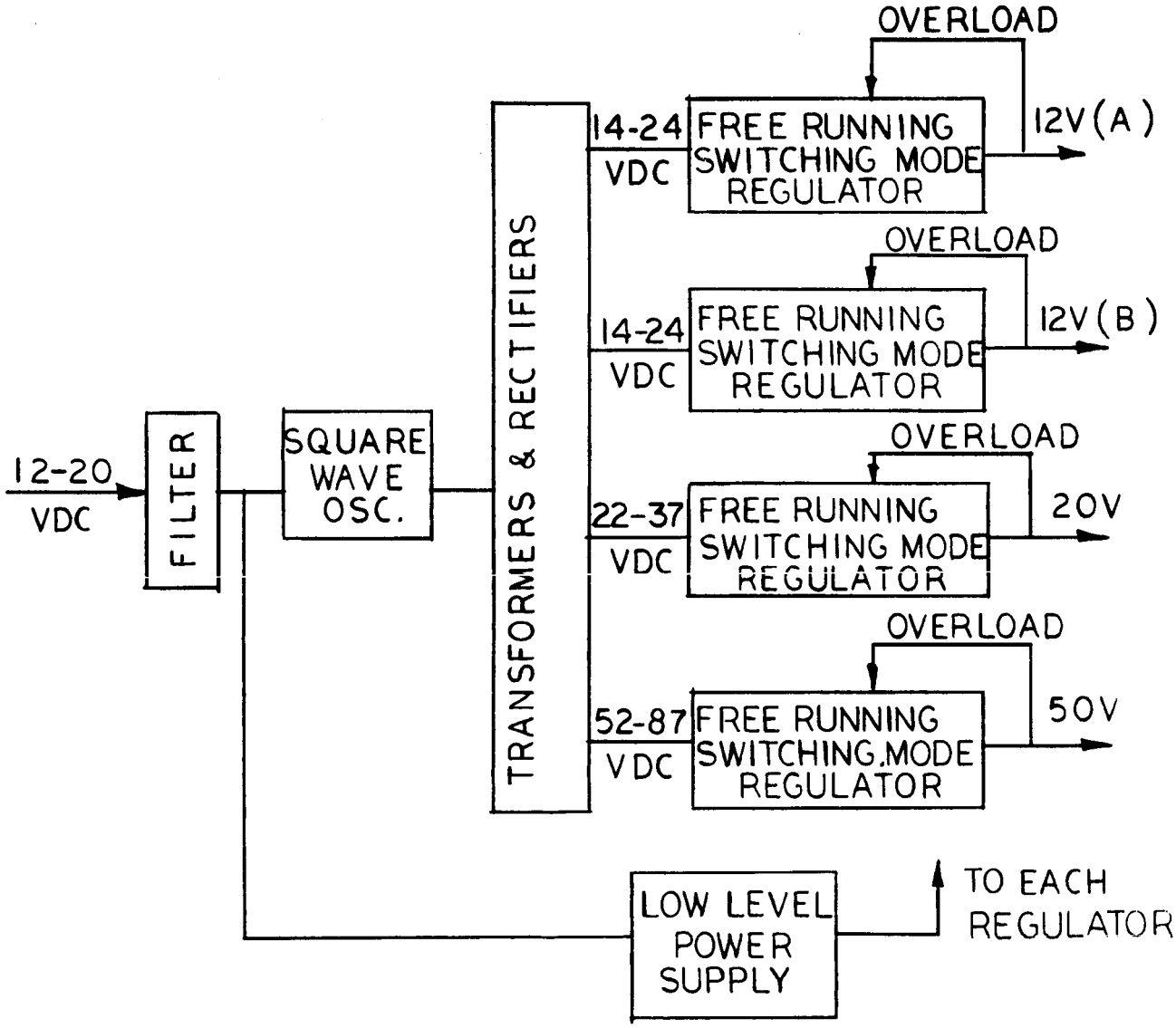


FIGURE 1. BLOCK DIAGRAM DC/DC CONVERTER
MODEL EMCR 131A.

I. INTRODUCTION

This is the final report describing an effort to advance the state of the art of DC/DC power conversion. These advances are proved by the development of a Model EMCR131A DC/DC Converter by optimizing the existing Model EMCR131 design.

The Model EMCR131 DC/DC Converter is the result of a previous research and development study program under NASA Contract NAS5-3470, which was completed as described in EM Report 1598 dated May 1, 1965, titled Final Report for Research and Development on DC/DC Converter Engineered Magnetics Model EMCR131. This model was designed for high efficiency and high reliability operation from a solar cell/battery combination power source. It provided 59 watts output from four regulated, isolated, short circuit and overload protected (excepting the 50 VDC) outputs. The Model EMCR131A is designed for ultra high reliability and is overload protected on all outputs. For a block diagram of the Model EMCR131A, see Figure 1.

II. REQUIREMENTS

The Primary purpose of the investigation is to improve the state of the art of DC/DC power conversion. These improvements were tested by fabricating a breadboard to a particular specification.

The input voltage is normally 19.6 volts DC but might vary between 12 and 20 volts DC. This input is converted to four isolated outputs of 12, 12, 20, and 50 volts DC. The outputs are to remain within 1/2 percent of the nominal voltage for all conditions of input voltage, load power (12 to 60 watts), and temperature ($-10^{o}C$ to $+60^{o}C$). The output ripple is to be held quite low (20 millivolts peak-to-peak on the 50V output, 10 millivolts peak-to-peak on the other outputs) although unclassified noise not included in the ripple may be somewhat higher (100 millivolts peak-to-peak on the 50V output and 50 millivolts peak-to-peak on the other outputs). Two dynamic regulation conditions were specified; a shift of input voltage between 12 and 20VDC with a 10 millisecond rise time, and a step load change between minimum and maximum load on either of the 12VDC outputs. Under either of these dynamic conditions, the outputs are not to change by more than 1/2 percent from their values before these conditions are applied and are to recover within 10 milliseconds to the normal regulation range.

Efficiency is to be 85 percent at full load and 80 percent at light load. All outputs are to be protected against overload by current limiting at about 150 percent of normal full load and are to recover when the overload is removed.

The unit is to be highly reliable and designed to operate in space for 30,000 hours or longer with no failure and negligible drift. Redundancy and fail-safe techniques are to be used to achieve this goal.

III. DESIGN

A. Configuration

The basic requirements of the system are voltage conversion, isolation, and regulation. Figure 1 is the block diagram of the approach used. Conversion and isolation are accomplished by a transistor oscillator and transformer with four outputs of somewhat higher voltage than the required regulated outputs. Regulation is then accomplished by four transistor regulators which reduce these voltages to the required levels and maintain them there regardless of variations of line and load.

Several other basic configurations were considered, but the one chosen is particularly straightforward. The ± 1/2 percent regulation required over a wide range of loads dictates the use of separate output regulators. Previously, the low output ripple specification and transient load requirement could only have been met by using four linear series regulators. Such regulators dissipate large amounts of power at high input voltage. Therefore, some form of high efficiency switching-mode pre-regulator would have to be added either before or after the converter. In this study, however, switching-mode regulators were developed with such low output ripple that they could supply the final regulation directly. The simple configuration that results is particularly efficient because the current must pass through only three semi-conductors; (1) a saturated transistor in the oscillator, (2) a rectifier, and (3) either a saturated transistor or a diode in the regulator. The oscillator uses a very efficient type of current drive and the regulators have redundant low level sense circuits and redundant current limiting.

B. Converter

The converter consists of a square wave transistor oscillator driving a toroidal transformer with four power outputs, four bias outputs, and the associated rectifiers. The transistors

operate in a switching mode in which they are normally fully on or fully off, and thus dissipate little power. The converter must operate over a very wide range of input currents for two reasons. First, of course, the loads themselves may vary over a range of 5:1. Second, the switching-mode regulators tend to draw a constant input power when feeding a constant load. Thus, input current increases as input voltage decreases. These two effects cause the input current to the converter to vary from approximately 0.7 amps (minimum load, high line voltage) to approximately 7.2 amps (50 volt output overloaded almost to the limiting point, other outputs at full load, and low line voltage). In order to operate efficiently over this range, a current driven square-wave oscillator circuit is used as shown in Figure 2.

This circuit is started by a separate unijunction transistor (not shown) which is effectively removed from the circuit when oscillation is achieved. With one transistor on (say Q102) the current supplied to the base is determined by the collector current and the turns ratio of the saturable transformer T101. This small transformer has a turns ratio of approximately 23:1 which provides the base with enough current to guarantee saturation but never delivers an excessive base current. The voltage on the base winding is $V_{be\ (sat)}$ of Q102 while the voltage reflected to the collector circuit is only one twenty-third of this. The opposite transistor (Q103) is held off with $-V_{be\ (sat)}$ on the base. Eventually the core of T101 saturates and current is drawn from the base of Q102 for a few microseconds (the storage time) after which it turns off. As the collector current of Q102 falls, T101 comes back out of saturation and applies positive voltage to the base of Q103, which turns on and remains on until T101 saturates again.

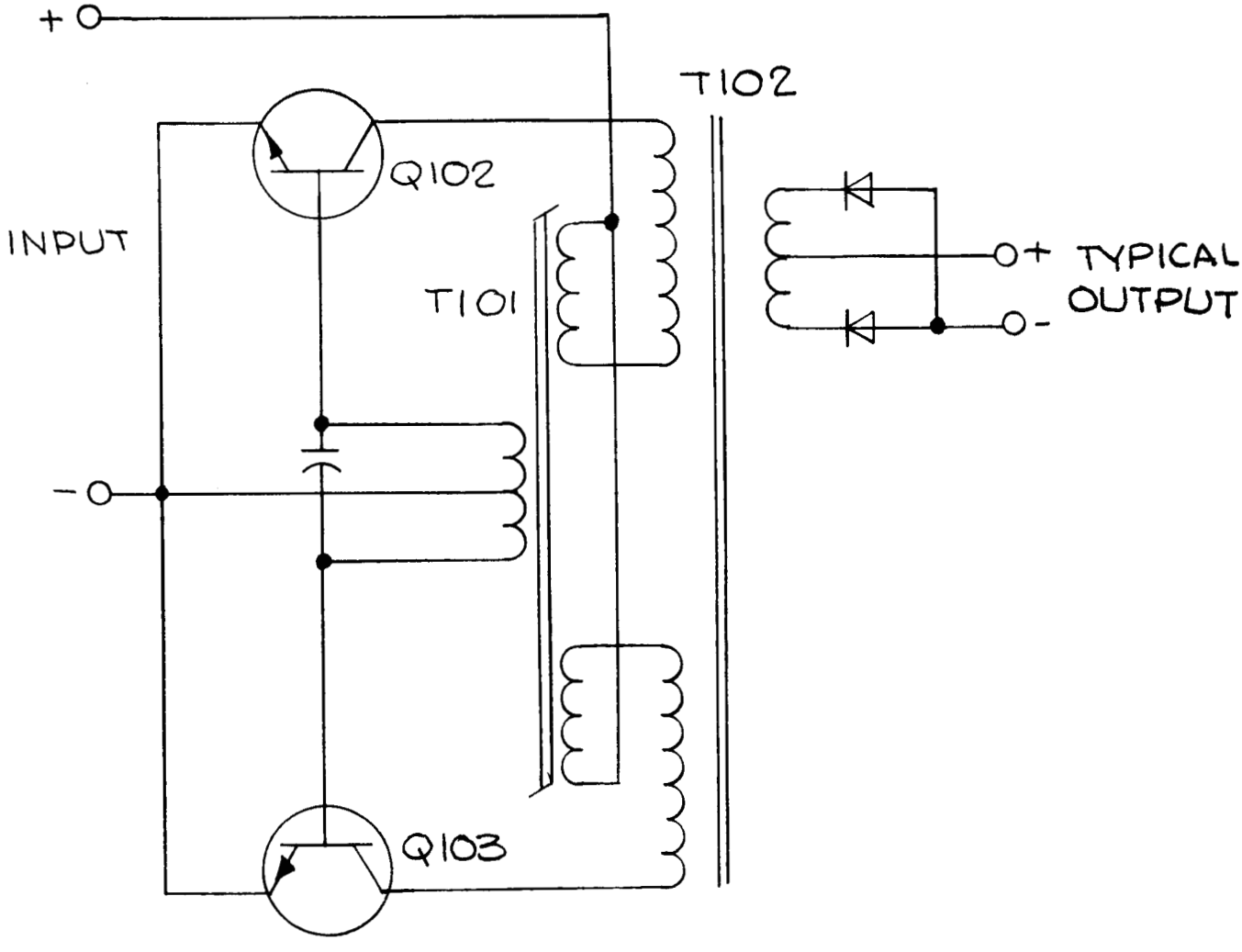


FIGURE 2. CURRENT DRIVEN OSCILLATOR.

The circuit has two main advantages; (1) the base drive is never excessive even under widely varying load conditions, and (2) both transistors are never on at the same time (not even for the transistor storage time as in some circuits). The frequency is fairly constant at approximately 5 KHz, which is both an advantage and disadvantage compared to some voltage-driven circuits in which the frequency is proportional to input voltage. In the current driven circuit, T102 is designed to support the highest input voltage at 5 KHz and thus could be operated at lower frequencies when the input voltage is low. Lower frequencies would be desirable from an efficiency standpoint. On the other hand, the input ripple filter must be quite heavy to filter even the 5 KHz and would have to be much larger if the frequency were allowed to decrease.

Transformer T102 does not saturate and is wound on a core of low-squareness permalloy which has the advantages of low coercive force (for low core loss) and of the ability to tolerate limited assymetrical drive.

The efficiency of the converter under various conditions is shown in Figure 3.

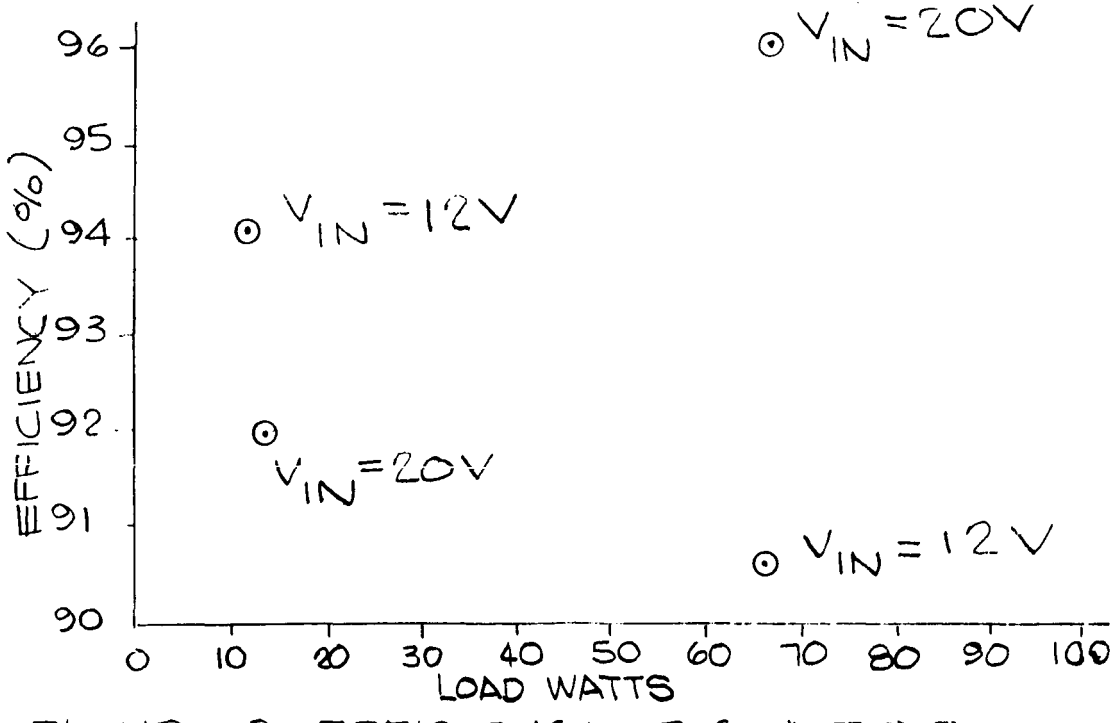


FIGURE 3. EFFICIENCY OF CONVERTER.

At high input voltage (the usual condition) the efficiency increases as the load increases while the opposite is true at low input voltage. This unusual effect may be explained in terms of the predominant type of loss under each of these conditions. The core is driven closest to saturation at high input voltage. Therefore, core loss is highest under this condition and predominates over other losses. Since core loss is constant with variations in load, the efficiency increases as the load power is increased. At low input voltage, core loss is smaller (about 12/20 of the loss at high input voltage) while the input current is larger (about 20/12 as large at the same load power). Also, the transistor saturation voltage is a larger percentage of the input voltage and rectifier voltages are larger percentages of the output voltages. This means that the transistor saturation and rectifier voltage drops predominate at low input voltage. Both the magnitude of the voltage drops and the current through them increase as the load power is increased, so efficiency goes down. This effect is minimized by using high current rectifiers which have lower voltage drops than rectifiers of normal rating.

A voltage-driven converter of comparable weight might be expected to have efficiency equal to the current driven converter only under one optimum combination of input voltage and load power.

C. Switching-Mode Regulators

1. Description

In order to meet the low ripple and dynamic load requirements, a conventional design would necessitate a series regulator operating in a linear mode. However, such regulators dissipate large amounts of power, especially at a high input voltage. A switching-mode regulator similar to Figure 4 is more efficient.

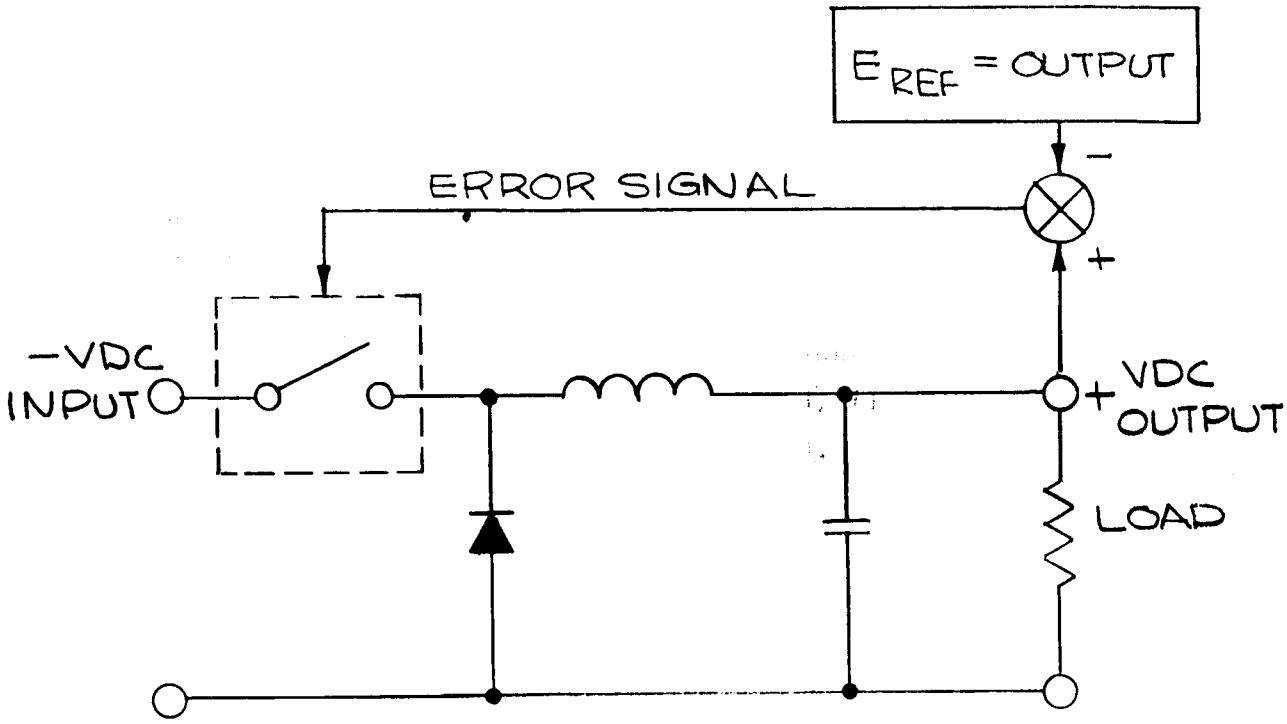


FIGURE 4 SWITCHING-MODE REGULATOR.

In this type of regulator a transistor is used as a switch to produce a series of pulses with an amplitude equal to the full input voltage. This train of pulses is then passed through a filter where it is reduced to the DC component of the train. This DC component is compared to a reference voltage and the resulting error signal controls the duty cycle of the pulse train. Switching-mode regulators were previously used only for high ripple applications. However, a switching-mode regulator with low ripple was developed during the course of this study.

The duty cycle of the pulse train may be controlled in a number of ways. A free-running switching-mode regulator technique (Patent pending) in which the switch is controlled directly by the error signal, has several advantages over other methods.

The ripple output of any switching-mode regulator is a function of the frequency (higher frequency gives lower ripple but also lower efficiency) and the input voltage. Since the free-running regulator operates from its own ripple, that ripple remains fairly constant. The frequency adjusts itself to the minimum necessary for the required output ripple at a given input voltage. A typical plot of these parameters is shown in Figure 5. A constant-frequency type regulator would have to run at the highest frequency in order to meet the ripple specification at high input voltage, but would far exceed the specification (at the cost of efficiency) at low input voltages. The free-running switching-mode regulator also has an advantage in that it operates well over the wide range of load currents required (30:1 on two of the outputs) and, indeed, even at no load.

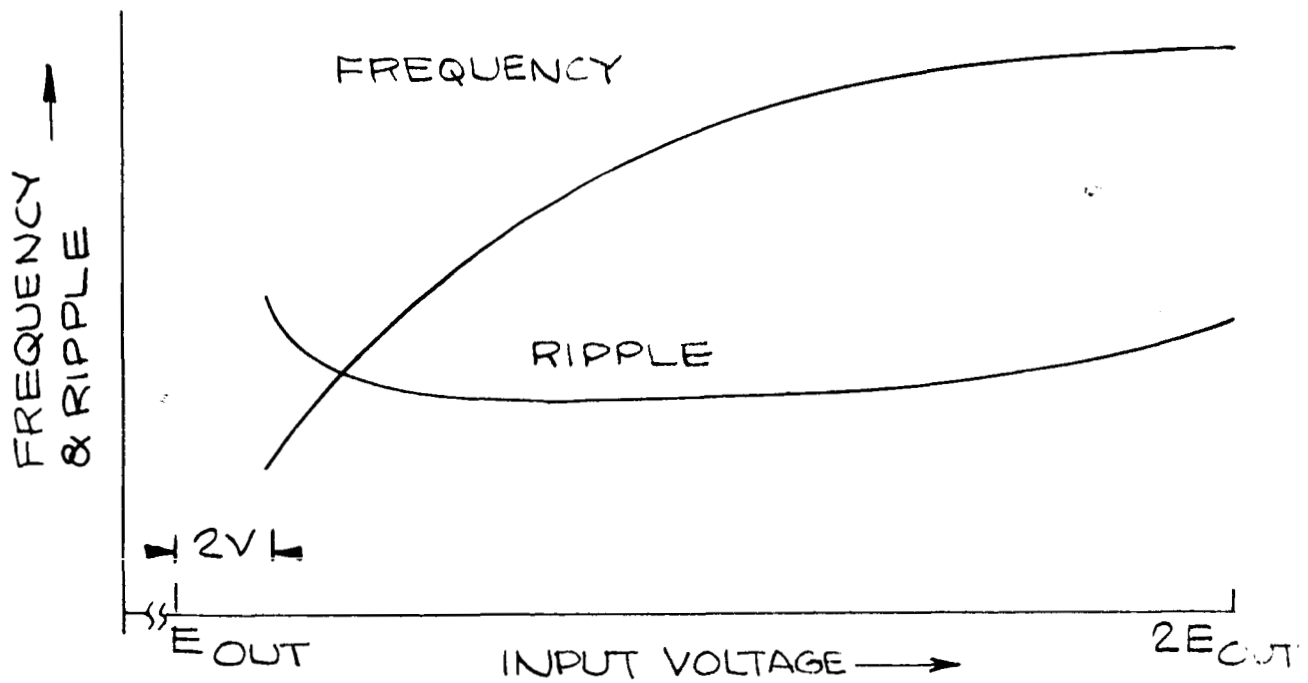


FIGURE 5. FREQUENCY AND RIPPLE OF FREE-RUNNING SWITCHING-MODE REGULATOR.

2. Analysis

Although the free-running switching-mode regulator is physically a fairly simple circuit, the operation is more complicated than one might expect. In order to improve the ripple and dynamic load response of the free-running switching-mode circuit, and to optimize it with respect to weight, size, and efficiency, an analysis aimed toward a better understanding of the circuit was undertaken.

The analysis of the circuit (detailed in the appendix) revealed a number of interesting aspects:

a. The quality of the capacitance is critical. The product, $R_c C$, of the series resistance and the capacitance must be small, or a large filter will be required.

b. The response time of the feedback network is critical even though it is small compared to the period of the pulse train. The greater the turn-on time T_{on} and the turn-off time T_{off} (primarily the storage time of the power transistor), the larger the physical and electrical size of the required filter. In fact, if $T_{on} + T_{off}$ exceeds $2R_c C$ the free-running switching-mode regulator cannot be designed to be stable no matter how large the filter used.

c. The hysteresis (d) of the feedback network is critical. The peak-to-peak ripple is often only slightly larger than d, but under some conditions the feedback circuit may "ring" up to values many times d.

To verify the final equations of this circuit analysis, a 12V free-running switching-mode regulator was constructed using a low-storage-time transistor (Fairchild FT34B), a low resistance capacitor, and an integrated circuit feedback amplifier. For controlled low hysteresis (d) the high gain integrated circuit operational amplifier used positive feedback as illustrated in Figure 6.

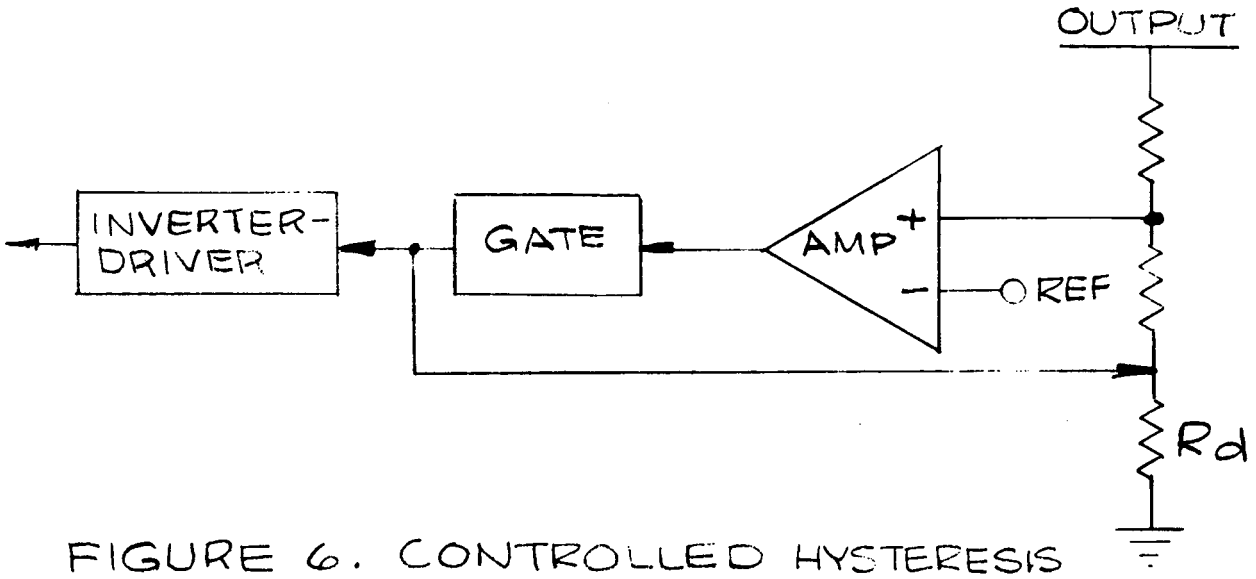


FIGURE 6. CONTROLLED HYSTERESIS FEEDBACK AMPLIFIER.

This circuit had less than 0.5 MV of hysteresis, open loop, making the circuit quite stable when R_d was adjusted for 3.0MV hysteresis. This feedback technique was later incorporated on all free-running switching-mode regulators used in the final breadboard.

The circuit parameters were:

d	= 3mV	E_{in}	= 24.0V
R_c	= 0.015Ω	E_{out}	= 12.0V
C	= 800μF	T_{on}	= 1.7μsec
L	= 1.0 mH	T_{off}	= 3.85μsec

The results were:

	Inductor current (peak-to-peak)	Ripple voltage (peak-to-peak)
Calculated	0.30 Amperes	5.0MV
Measured	0.28 Amperes	4.9MV

Current and voltage waveforms also had the shape predicted by the analysis.

With the analysis verified, free-running switching-mode regulators were then designed for the four converter outputs. The block diagram is shown in Figure 7. All outputs are current limited at a mini-minimum of 150% of full load and all critical low level circuits (i.e. comparators, references, and current limiting) are redundant for high reliability.

3. Redundant Voltage Sensing

Each free-running switching-mode regulator is controlled by three sense modules operating in a best-two-out-of-three or "majority" arrangement as shown in Figure 8. Each sense module receives the output voltage, reduces the voltage by means of a temperature-stable resistive divider and compares the voltage to a temperature-stable reference. The difference (or error) signal is then amplified by an integrated circuit operational amplifier and a gate providing a bistable output of "1" or a "0".

The inverter-driver reacts in favor of two or more of the sense modules. That is, if the output of the first two sense modules are "1"s but a failure has occurred in the last sense module so that its output is a "0", the inverter-driver sees this as a "1". Any single sense module can fail in either direction and the free-running switching-mode regulator will still function.

Under normal (no failure) operation, regulation is especially good because the poorest sense module is always ignored.

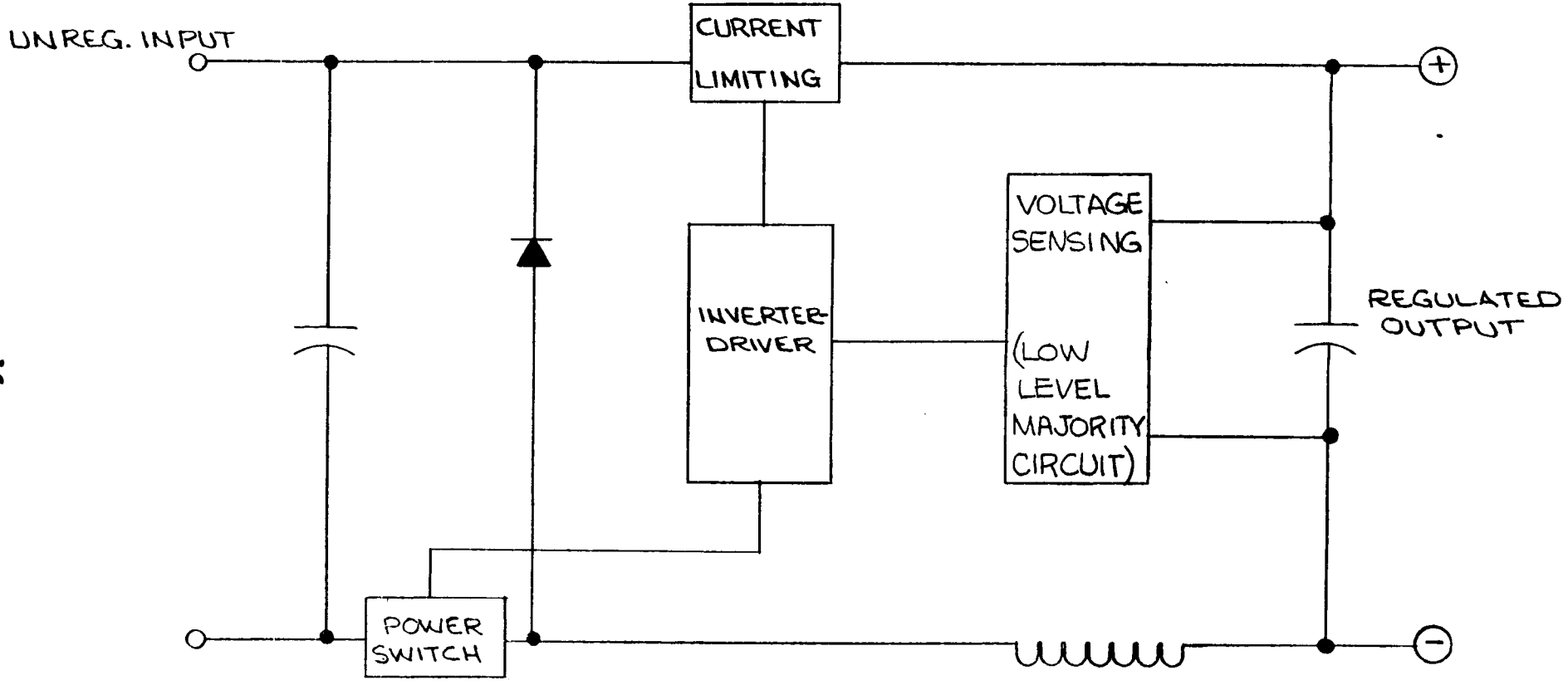


FIGURE 7. BLOCK DIAGRAM, TYPICAL FREE-RUNNING SWITCHING-MODE REGULATOR.

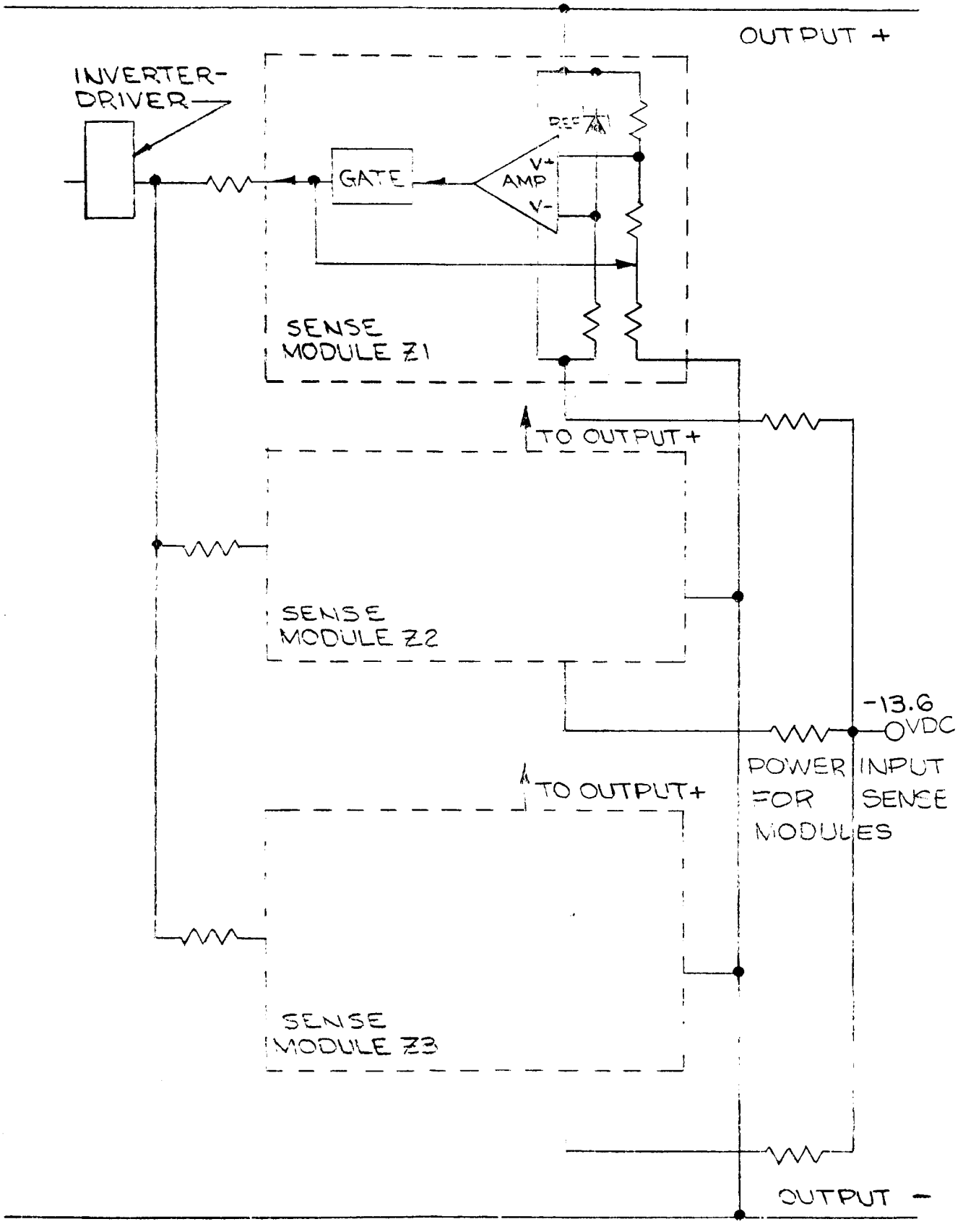


FIGURE 8. REDUNDANT VOLTAGE SENSE CIRCUIT.

Suppose that at -20°C, the output of sense module Z1 of the 50V free-running switching-mode regulator switches when the regulator output is at 49.910 volts. At the same temperature, sense module Z2 might switch at 49.955 volts and sense module Z3 at 49.963 volts as shown in Figure 9. The inverter-driver would then switch when the output was 49.955 volts, the middle of the three. At 25°C, sense module Z1 might switch at 50.000 volts, sense module Z2 at 50.200 volts and sense module Z3 at 49.980 volts. At this temperature, the free-running switching-mode regulator would operate at 50.000 volts, again the middle of the three. This effect also operates, of course, for variations with line voltage and load as well as with temperature. Even if one sense module's reference were to drift drastically, regulation would still be unimpaired. Thus, if in the above 25°C example, sense module Z1 switched at 45.000 volts (due to a non-catastrophic reference failure) the unit would still regulate in specification at 49.980, the middle of the three.

Figure 9 actually shows normalized experimental data. When all three sense modules are adjusted to operate at nearly the same sense voltage, it is often difficult to tell which sense module is in control of the power stage. For testing purposes, each sense module was adjusted to a different voltage (approximately 49, 50, and 51V) and each in turn was placed in control by simulating a failure in another sense module. The effect of varying the temperature could then be observed individually and normalized to the settings that might actually be used. The normal output would be the middle line (shown solid), while the dashed lines would be the limits in the event of failure in one sense module.

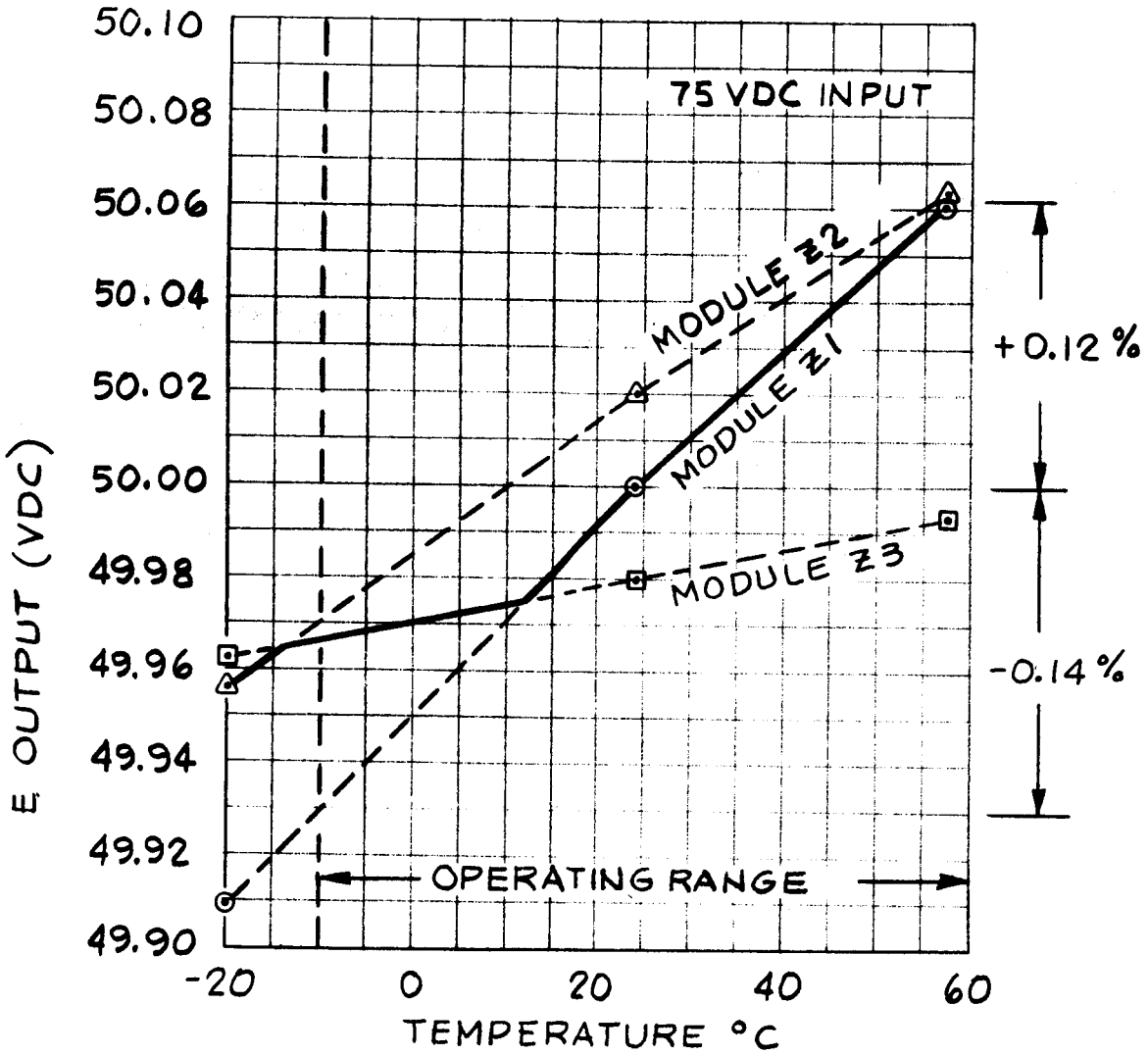


FIGURE 9. NORMALIZED OUTPUT VOLTAGE VS. TEMPERATURE, 50 V FREE-RUNNING SWITCHING MODE REGULATOR.

The transfer function (voltage into inverter-driver vs sensed output voltage) is shown in the oscilloscope trace, Figure 10. This trace was obtained by applying 50VDC and about 40 MV p-p AC to the sense leads of the three sense modules (between OUTPUT + and OUTPUT - in Figure 8) and to the horizontal axis of the oscilloscope. The vertical axis is the voltage at the junction of the three summing resistors (with the inverter-driver disconnected). The threshold of the following stage is such that the unit normally operates in the middle loop (the one that intersects the threshold).

If any sense module were to fail (i.e., a full on or full off condition) there would be only two hysteresis loops, but one of them would cross the threshold. If, on the other hand, the threshold voltage were to drift below 2.0 volts or above 4.0 volts, the unit would still operate (though it would no longer be able to tolerate certain failures in the sense modules). Note that the hysteresis is the same for all three loops since it is determined only by the feedback resistors.

4. Redundant Current Limiting

All four converter outputs are current limited at 150% of rated load. The protection circuitry is the same for all converter outputs and is shown in Figure 11. Full redundancy (section A and section B of Figure 11) is used to guarantee that current limiting will never occur merely because of a failure in the current limiting circuits.

The current is sensed with a low value resistor and the resulting voltage is compared to the difference between two semiconductor junction voltages; a diode voltage, and a transistor base-emitter voltage. When the voltage

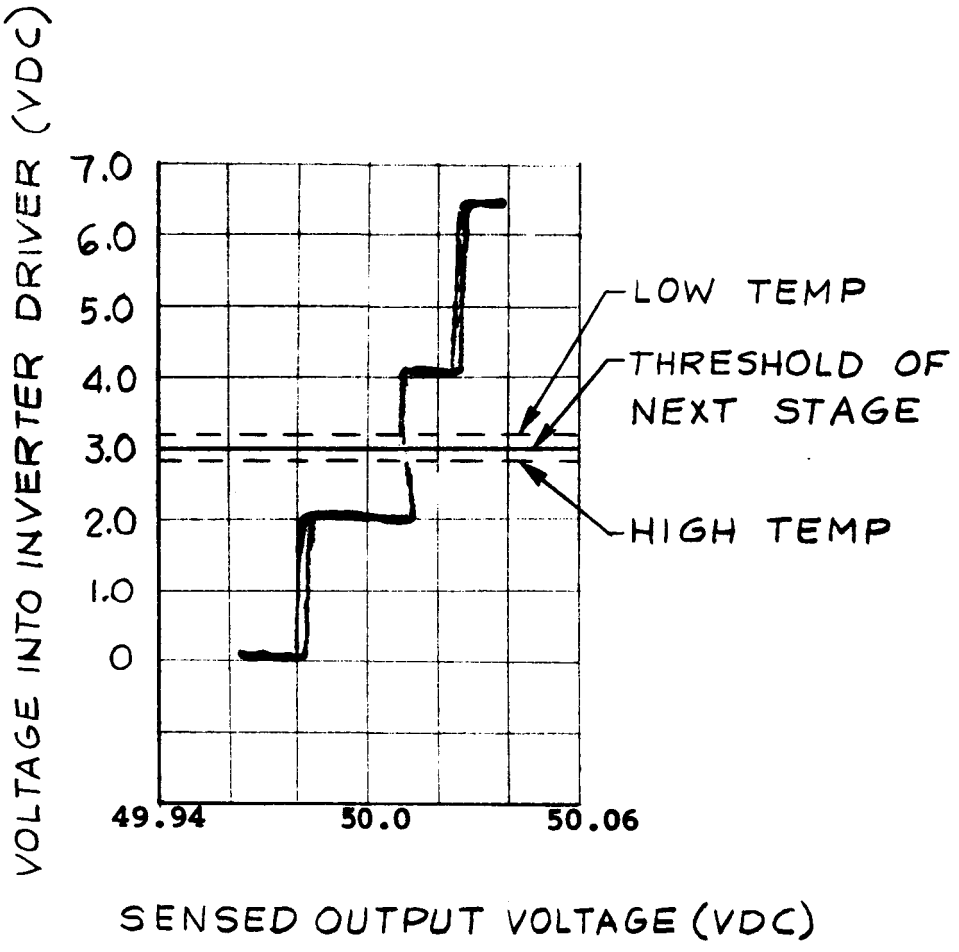


FIGURE 10. VOLTAGE INTO INVERTER DRIVER VS SENSED OUTPUT VOLTAGE.

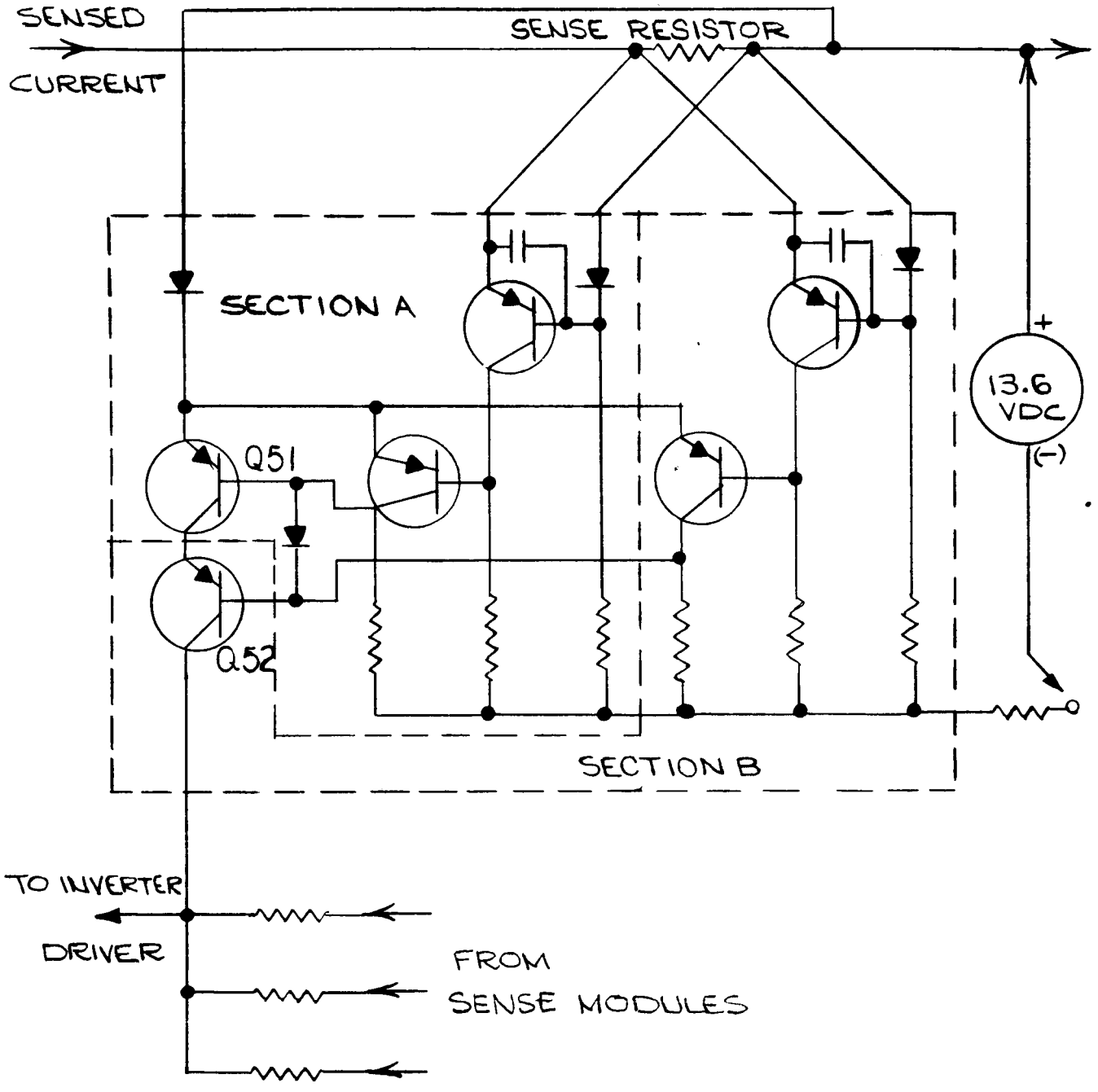


FIGURE 11. REDUNDANT CURRENT LIMITING.

When the voltage across the sense resistor (0.05 to 0.1Ω) reaches about 75 MV, Q51 and Q52 are turned on, holding the inverter-driver in an off condition until the current decreases. Since Q51 and Q52 are in series, they must both be on in order to cause the free-running switching-mode regulator to turn off.

While a failure in this redundant current limiting circuit might deactivate the protection, no single failure in Section A or in Section B could cause the unit to turn off prematurely. Thus the failure rate for the entire redundant current limiting circuit is reduced almost to the failure rate of the sense resistor only. (Loss of overload protection is not considered to be a failure).

If the two sensing sections A and B, are not adjusted to limit at exactly the same current, limiting occurs at the higher of the two. Each section can be individually observed by simulating a failure in the other, i.e., shorting Q51 or Q52 collector-emitter. Performance of the 50V free-running switching-mode regulator under these conditions is shown in Figure 12 and 13. Normal operation would be on the solid line, with the dashed line a lower limit if a failure should occur in the redundant current limiting circuit.

5. Component Evaluation

The analysis of the free-running switching-mode regulator circuit (see Appendix) indicated that if the $R_C C$ product of the capacitors is not small, a large filter (large LC product) is required to achieve low ripple. Unfortunately, high frequency $R_C C$ data is not available from most capacitor manufacturers. The usual measuring technique is an impedance bridge, but this gives erratic readings at high frequency when the capacitor is very large.

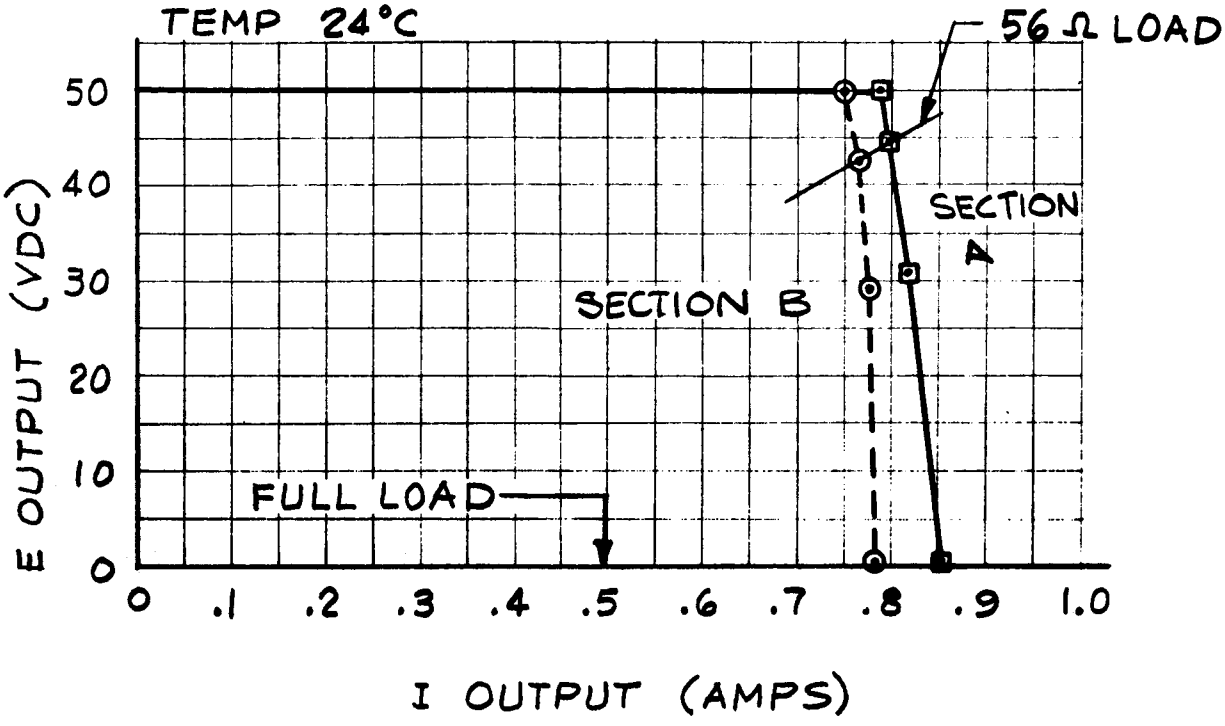


FIGURE 12. OUTPUT VOLTAGE VS OUTPUT CURRENT 50V FREE RUNNING SWITCHING MODE REGULATOR

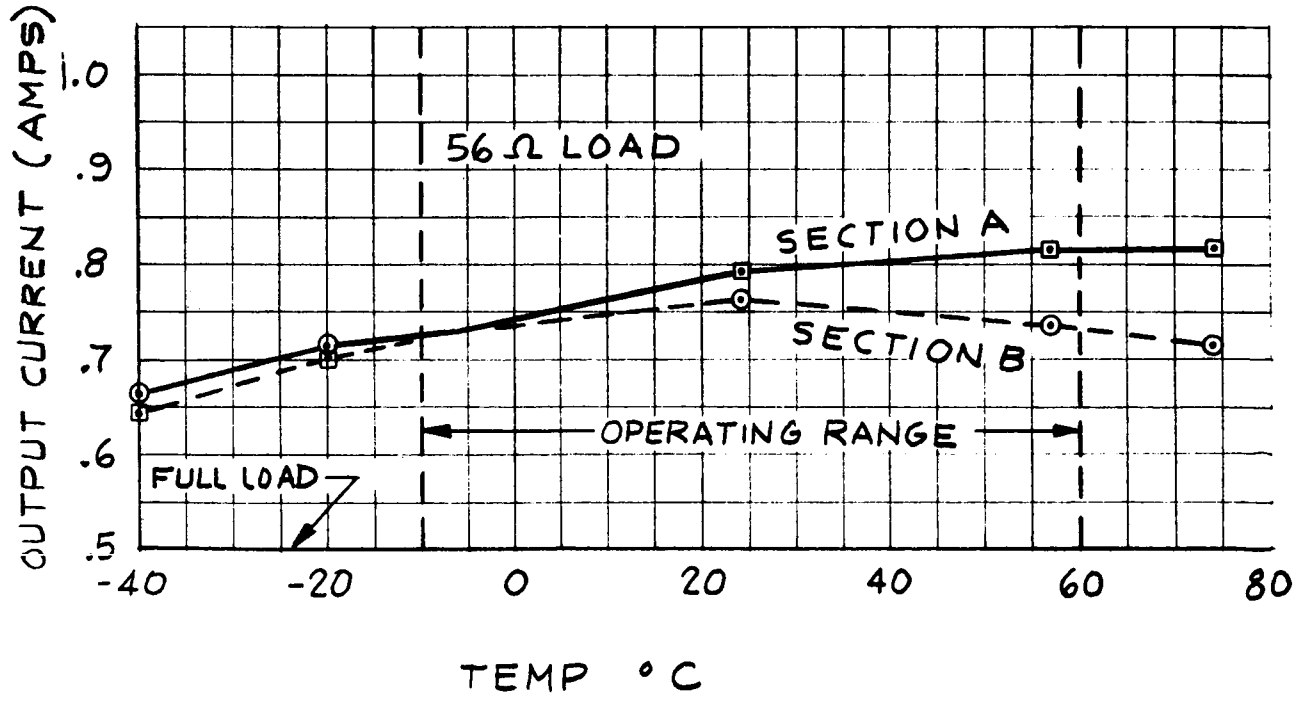


FIGURE 13. CURRENT LIMITING, 50V FREE RUNNING SWITCHING MODE REGULATOR.

A new test method was used to determine the R_cC at high frequency. The circuit is illustrated in Figure 14.

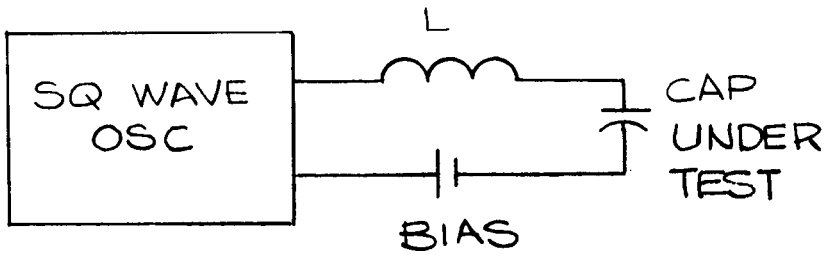
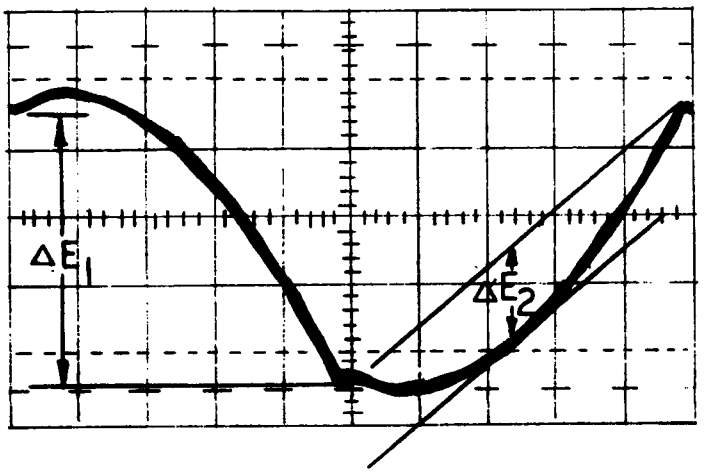


FIGURE 14. CAPACITOR TEST CIRCUIT.

The oscillator frequency is much higher than the resonant frequency of the inductance and the capacitor. Thus the circuit provides a triangle current into the capacitor to approximate the conditions found in the switching-mode regulator. The voltage across the capacitor is observed on an oscilloscope and C and R_c are measured directly on the screen, or from photographs of the trace as shown in Figure 15a. Figure 15b gives the equations used to calculate the R_cC product of a typical sprague 350 D capacitor from the oscilloscope photograph of Figure 15 a.

Typical data were taken on a variety of capacitors using this method and the results are given in Table I. The Hunter-Stanley WS series of capacitors appear to be excellent for this application, but reliability data is not complete.

The Sprague 350D series of solid tantalum capacitors were chosen for the 12 volt free-running switching-mode regulators. A bank of thirteen capacitors was required on each 12V regulator to meet the ripple and transient load specffications.



a. Capacitor voltage for 0.4A peak-to-peak triangle current at 10kHz

b. Analysis

$$R_c = \frac{\Delta E_1}{\Delta I} = \frac{8 \times 10^{-3} V}{0.4A} = 0.020\Omega$$

$$C = \frac{\int i dt}{\Delta E_2} = \frac{2.5 \times 10^{-6} \text{ Coul}}{2.8 \times 10^{-3} \frac{\text{Coul}}{V}} = 893\mu F$$

$$R_c C = 18\mu sec$$

FIGURE 15. TYPICAL MEASUREMENT OF R_c AND C AT 10kHz.

TABLE I. MEASURED CAPACITOR PARAMETERS.

TYPE, RATED C & RATED VOLTAGE AT 85°C/100°C	R_c (Ω) C (μF) R_cC (μsec)	FREQUENCY (KHz) 5	10	20
WS 140, 2200 μF 20 V/ 15 V (Hunter-Stanley)	R_c	.018	.014	.012
	C	1820	1560	1250
	R_cC	33	22	15
WS 141, 1600 μF 30 V/ 20 V (Hunter-Stanley)	R_c	.018	.015	.012
	C	1390	1250	960
	R_cC	25	18	12
WS 142, 1200 μF 50 V/ 30 V (Hunter-Stanley)	R_c	.020	.017	.015
	C	1185	1020	808
	R_cC	23	17	12
WS 145, 375 μF 100 V/ 65 V (Hunter-Stanley)	R_c	.025	.023	.020
	C	350	400	390
	R_cC	9	9	8
350 D 1000 μF 20 V (10x100 μF in parallel) (Sprague)	R_c	.025	.020	.017
	C	870	893	782
	R_cC	22	18	13
29F 1000 g 36 1000 μF 52 V/35 V (old model) (G.E.)	R_c	.035	.033	.030
	C	952	1250	834
	R_cC	33	41	25
29F 3272 G 18 1000 μF 52 V/35 V (newer model) (G.E.)	R_c	.103	.097	.085
	C	833	590	416
	R_cC	86	57	35
16K 361 95 μF 75 V/50 V (G.E.)	R_c	.48	.40	.37
	C	100	83	83
	R_cC	48	33	32
137D 270 μF 15 V (Sprague)	R_c	.368	.288	.245
	C	167	125	93
	R_cC	60	36	23

Sprague 350D capacitors are not available at voltage ratings above 50V, therefore General Electric 29F and 16K capacitors with higher voltage ratings are used for the 50V free-running switching-mode regulator. Although the R_cC products of these capacitors are poor, fewer capacitors are needed. This is possible because there is no transient load requirement for either the 50V or the 20V regulators, and pi-section filters could be used instead of single banks of capacitors. The ripple across the input capacitor of a pi-section filter may be quite high since the remainder of the filter provides considerable attenuation. This means that capacitors with relatively poor R_cC products (but adequate voltage rating) can be used and relatively few capacitors are required. The only disadvantage is slow transient load response and this is not a problem on the 20V and 50V regulators.

The free running switching-mode regulator analysis also shows that the switching time of the power transistor must be short if the filter is to be small. A number of transistors were tested for switching time in a circuit that simulates the free running switching-mode regulator and the results are summarized in Table II. The Fairchild FT-34B transistor was chosen for the critical 12V regulators because it has very fast switching times and a very low saturation voltage drop. A Solitron 2N2658 was used for the 20V regulator which, with its pi-section filter, is not so critical as to switching time. A Solitron STD7A23 was used for the 50V regulator because of its high voltage rating (140V V_{ceo}).

TABLE II. TRANSISTOR SWITCHING TIMES.

MANUFACTURER	TYPE	I.D. NO.	t_{rise}	t_{fall}	$t_{storage}$
CONT. DEV.	855M-3	2G21003	.08	.18	1.6
	855M-3	BT4488	.06	.28	2.4
TRW	855M-3	1535	.05	.11	2.2
	855M-3	1530	.05	.12	2.1
SOLITRON	2N2214	X	.06	.15	4.8
	MHT7403	X	.07	.14	5.3
	MHT6313	X	.04	.12	2.6
	2N2658	BF3798	.04	.10	2.2
	2N2658	BR3594	.04	.14	2.4
	SES196	A	.06	.15	2.8
	SES196	B	.06	.15	2.8
FAIRCHILD	FT-7207B		.04	.025	0.8
	FT-7207B		.04	.025	0.7
	FT-34B		.03	.14	1.1
	FT-34B		.03	.16	1.4

6. Efficiency of Regulators

A survey was made of the power loss mechanisms in one of the free running switching-mode regulators (the 12V a) to locate the most promising areas for improvement. The transistor switching losses were found to be the largest single type of loss. It was observed that when the regulator switching transistor began to turn off, the voltage across the transistor rose from nearly zero to the full input voltage almost immediately, but the current did not fall substantially until some time later. This maintained the transistor at high power levels (although within rating) for approximately one microsecond causing 0.68 watts of power loss at 40KHz. Transistor base waveforms indicated that the transistor was slightly turning on again during the collector voltage rise. To counteract this effect, a kick winding on the inductor was used to switch the transistor base negative as soon as switching was started. This technique drastically reduced the power loss as shown in Figure 16. With the kick winding in place, most of the 12V regulator losses are divided almost equally among three types:

Losses at 20V input	Watts
Diode forward drop	0.27
Sense modules	0.23
Transistor switching	0.22

Regulator efficiency is excellent even at the high frequency used and with redundant sense and current limiting circuits. Efficiency of the 50V regulator (the best in this respect) is shown in Figure 17.

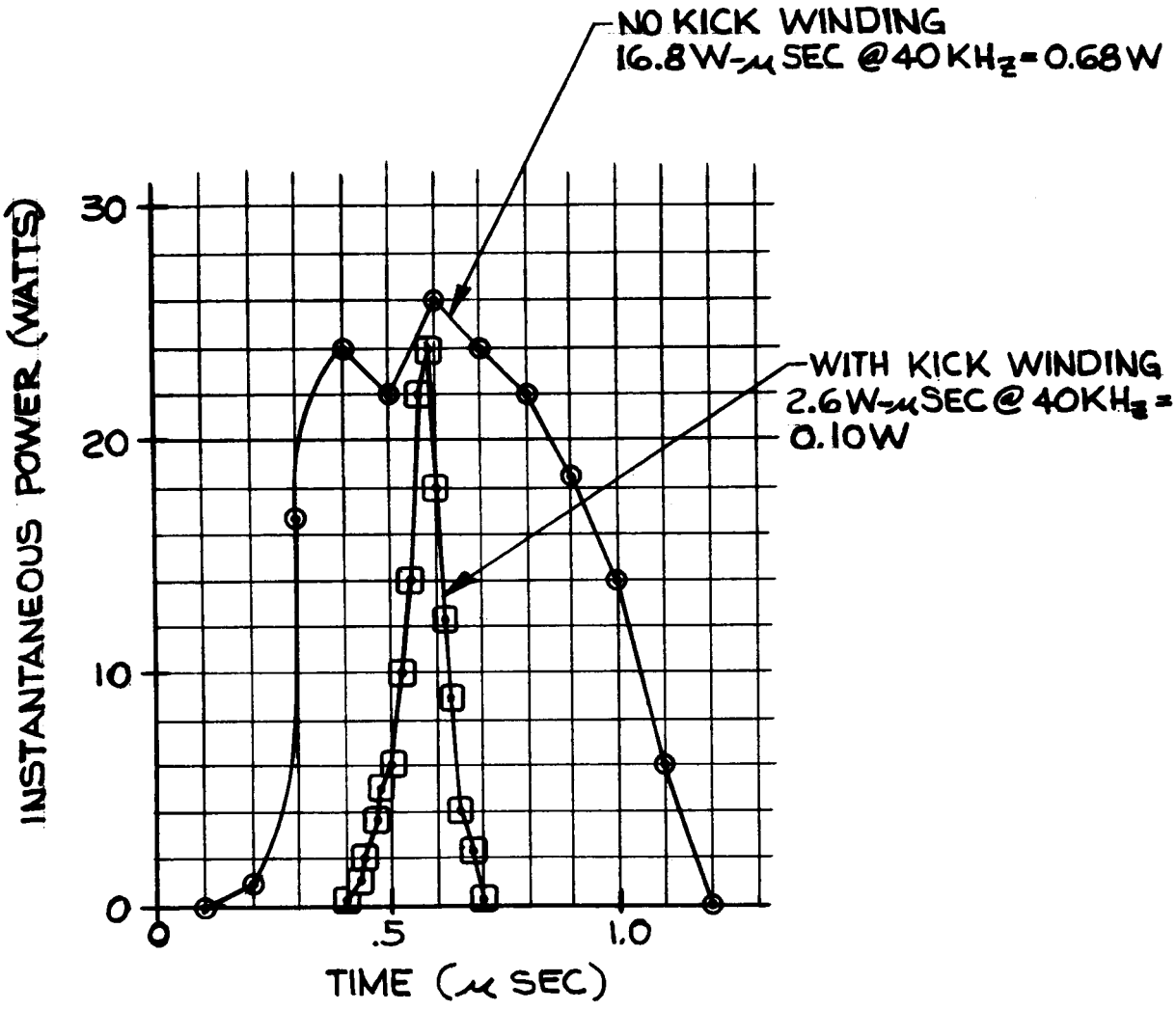


FIGURE 16.
POWER DISSIPATION IN REGULATOR SWITCHING TRANSISTOR AT TURN OFF.

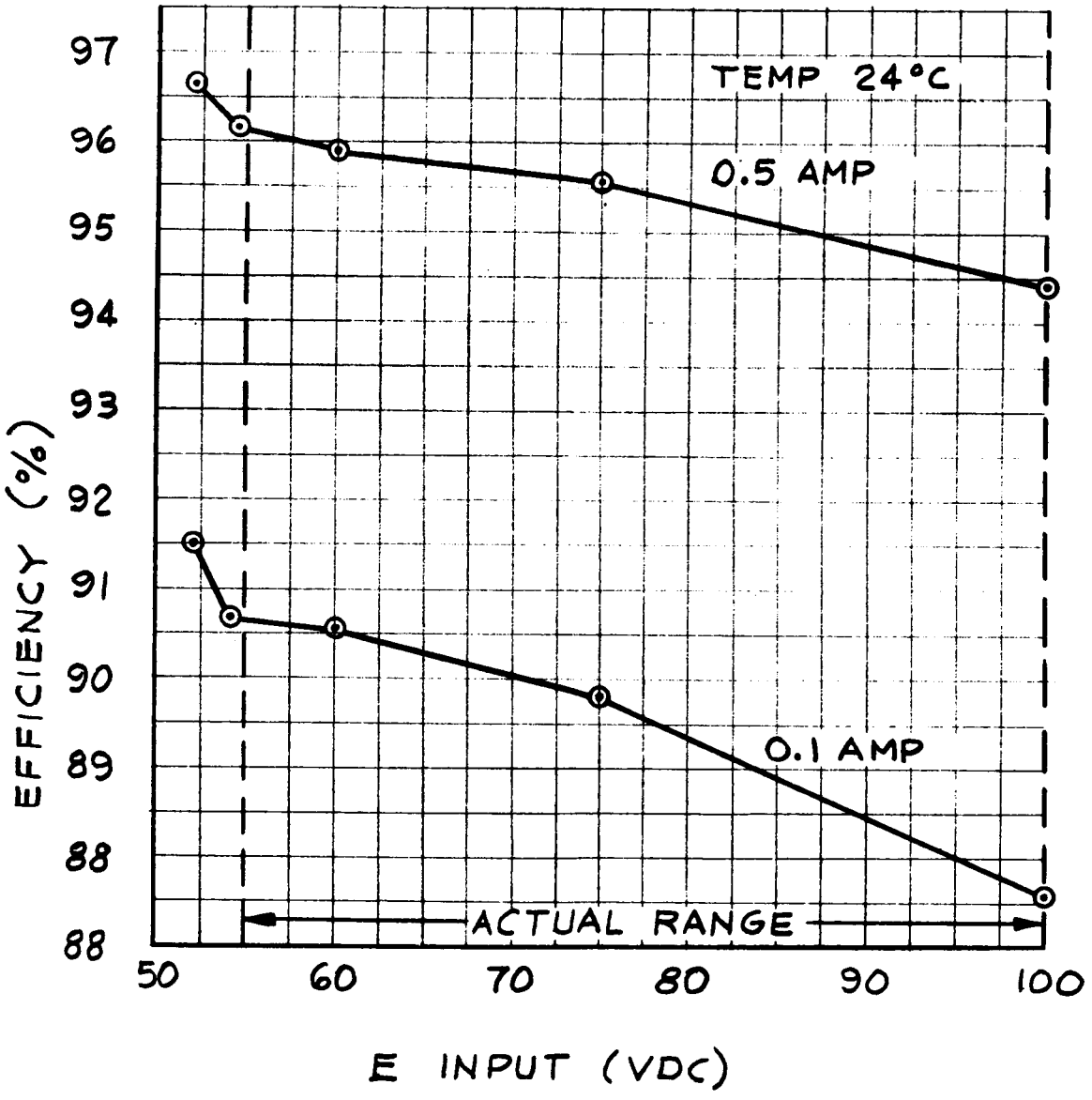


FIGURE 17. EFFICIENCY VS INPUT VOLTAGE 50V FREE RUNNING SWITCHING MODE REGULATOR.

D. Power For Low Level Circuits

Each of the redundant voltage sense modules require approximately 80MW of power at 12V, or a total of 240MW per output regulator. For the 12V, this power could be taken directly from the regulated output. To supply the voltage sense modules of the 20V and 50V regulators from their respective outputs would require resistive dividers. The power drawn from the 50V output for this purpose would be:

$$\left(\frac{50}{12}\right)^2 \quad (3 \text{ X } 0.08) \; = \; 4.17\text{W}$$

which is excessive.

To avoid this power drain, a separate, or auxilliary, power supply is used which provides regulated power for all the voltage sense modules in all the free running switching-mode regulators. This approach has two additional advantages; the outputs of the regulators are automatically started when power is applied to the voltage sense modules, and the auxilliary power supply can also provide power for the current limiting circuit.

This auxilliary power supply must, of course, be ultra-reliable. Complete redundancy is used. A failure anywhere in the auxilliary power supply could be tolerated without ill effect. The straightforward approach used for the auxilliary power supply, illustrated in Figure 18, is possible because the regulation need not be precise and the power involved is small. Two complete sections are operated in parallel. Each section consists of a very simple type of free running switching-mode regulator followed by a transistor square-wave converter. Diodes are used to couple corresponding outputs of the two sections to prevent a failure in one section from loading the other section. The inputs are fused to prevent a failure in one section from excessively loading the input line, and zener diodes are used to protect against any possible excessive voltage.

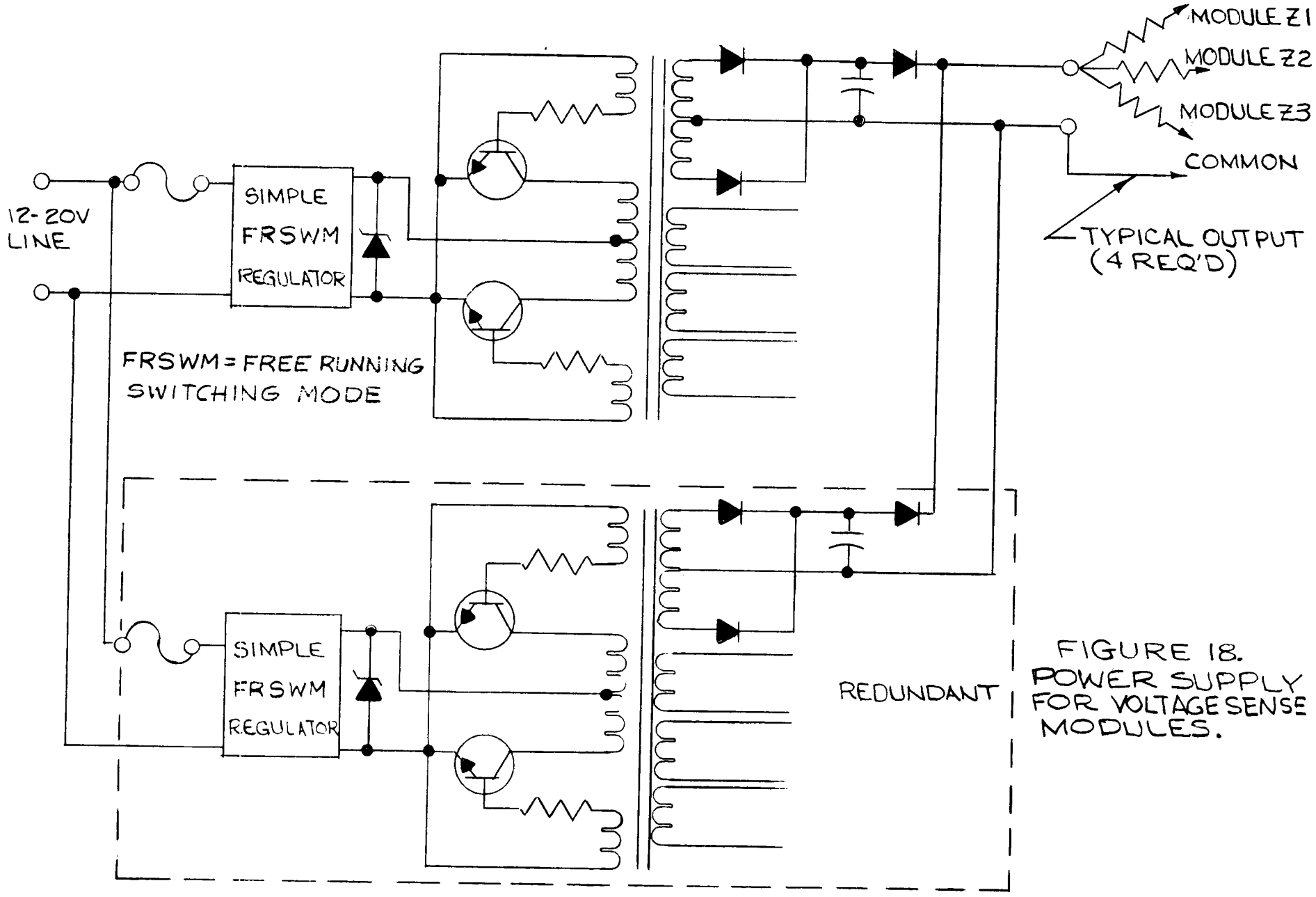


FIGURE 18.
POWER SUPPLY
FOR VOLTAGE SENSE
MODULES.

The four isolated outputs of the auxilliary power supply are nominally at 13.6V. This is reduced to about 12V and distributed to the voltage sense modules by a resistive network. This network limits the current. In the event of a failure of one voltage sense module in any free running switching-mode regulator, the failure could be tolerated without loss of power to the other voltage sense modules.

The regulation is very good under normal operating conditions, as shown in Figure 19. The output remains between 13.6V and 14.1V even if a failure occurs. This 0.5V maximum change would shift the power outputs by only 0.05%. Efficiency of the auxilliary power supply is approximately 60% when both sections are running and about 67% for either section alone. This efficiency would not, of course, be acceptable in a main power converter, but is quite reasonable in this application since the power involved in only 1.2 watts. Efficiency was traded for reliability to the extent that the failure rate of the auxilliary power supply is negligible in the overall reliability calculation. (See Section VI, Reliability.)

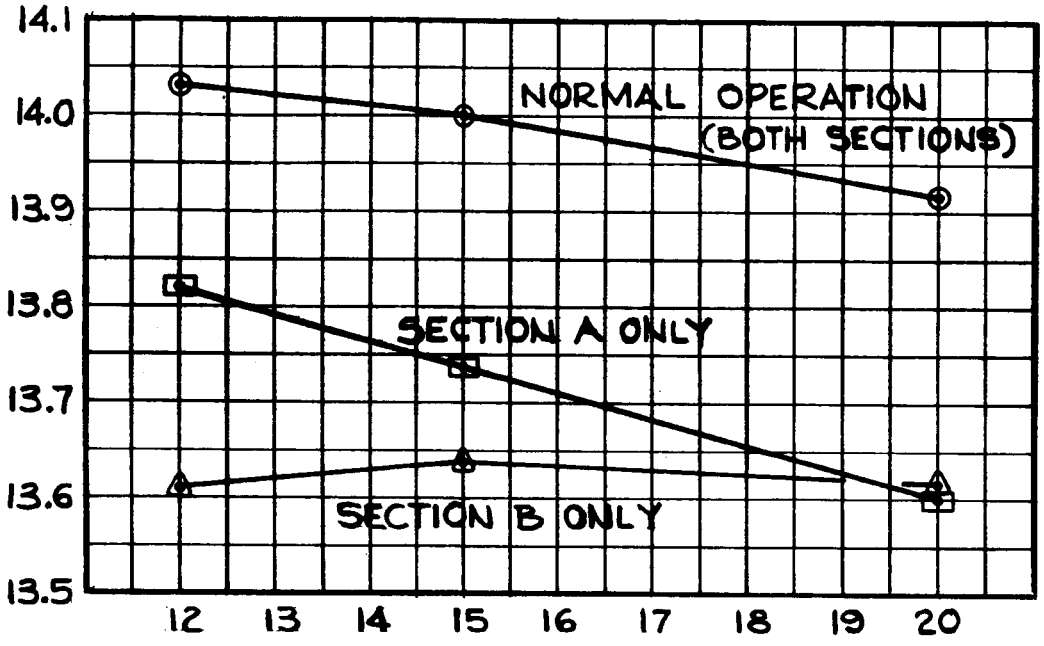


FIGURE 19.
VOLTAGE REGULATION OF AUXILLIARY POWER SUPPLY FOR REDUNDANT VOLTAGE SENSE MODULES (TYPICAL OUTPUT).

IV. PERFORMANCE

A. Output Voltage

1. Static Regulation

Each of the converter outputs remain well within the required ± 1/2 percent of their nominal voltages under all required conditions as shown in Table III.

	OUTPUT CURRENT (MA)	
	MINIMUM AT 12V INPUT AND AT -10°C	MAXIMUM AT 20V INPUT AND AT +60°C
CONVERTER OUTPUT		
12 (a)	500	1000
12 (b)	50	1000
20	25	500
50	100	500

TABLE III. INPUT, LOAD, AND TEMPERATURE CONDITIONS.

The output variations with each of these parameters are shown in Figures 20, 21 and 22. The favorable effect of redundancy is particularly noticeable for the 12V(a) output vs temperature (See Figure 22.) One voltage sense module of the free running switching-mode regulator is in control below 20°C, a second between 20°C and 30°C, and the third above 30°C. The worst case output voltages are summarized in Table IV.

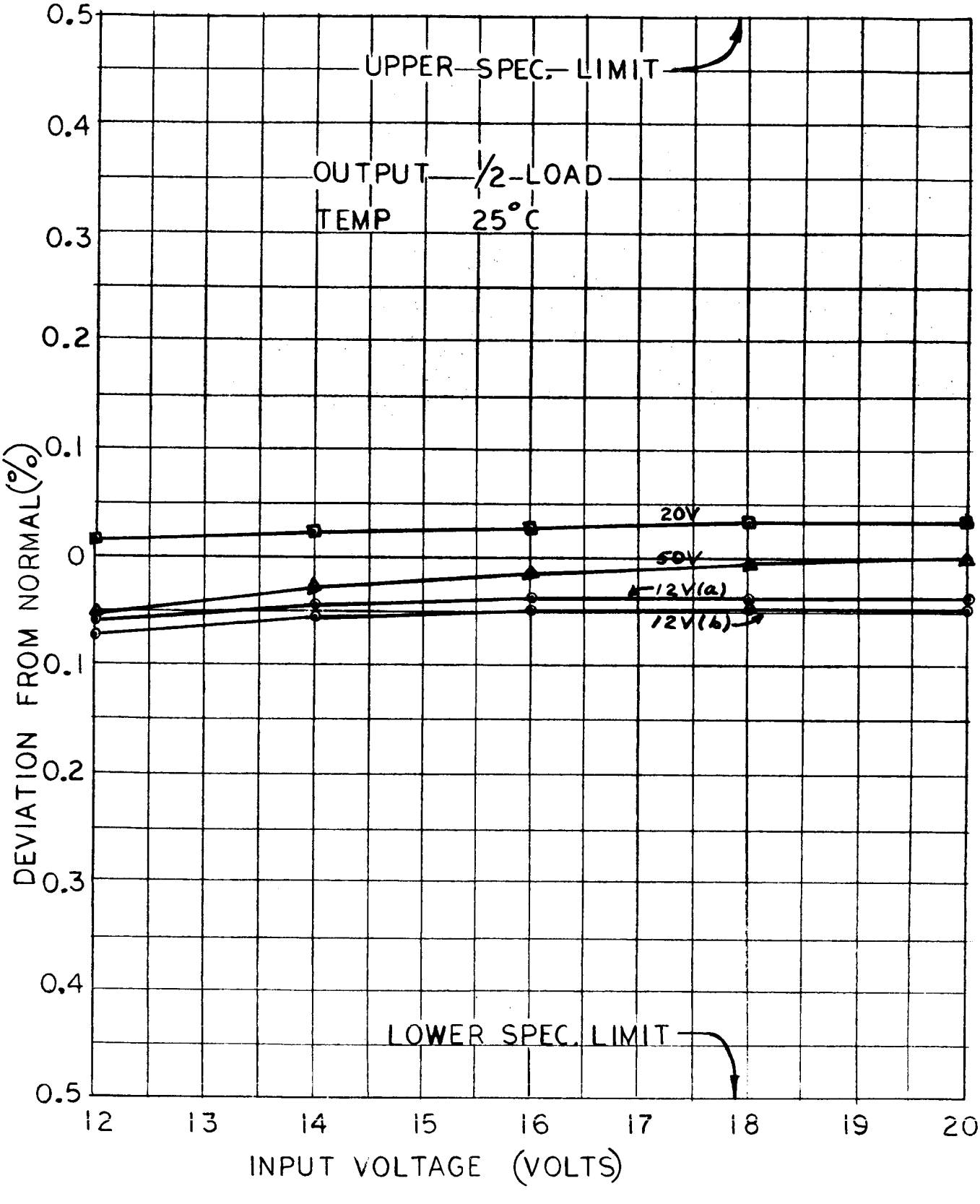


FIGURE 20. OUTPUT VOLTAGE VS INPUT VOLTAGE.

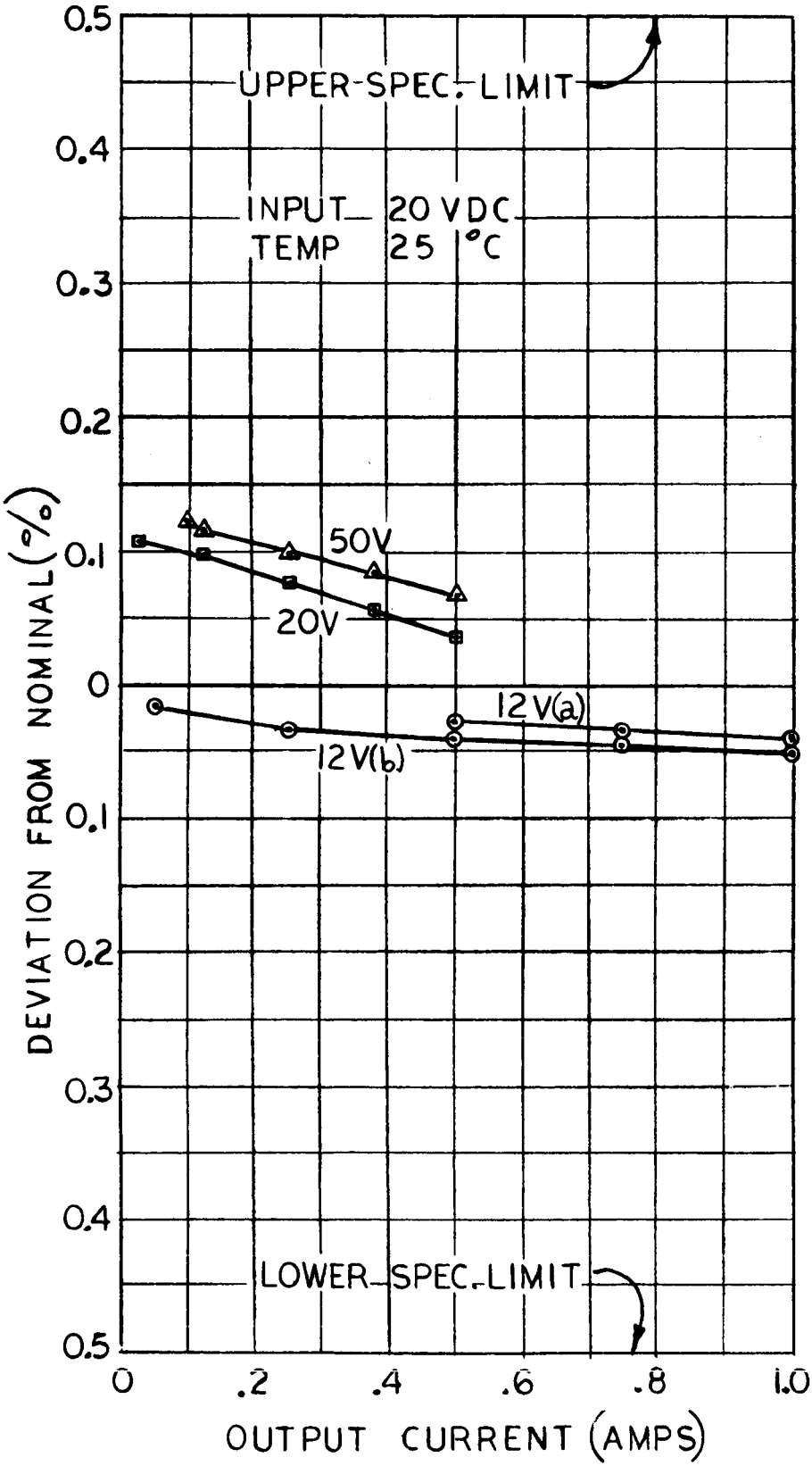


FIGURE 21. OUTPUT VOLTAGE VS LOAD CURRENT.

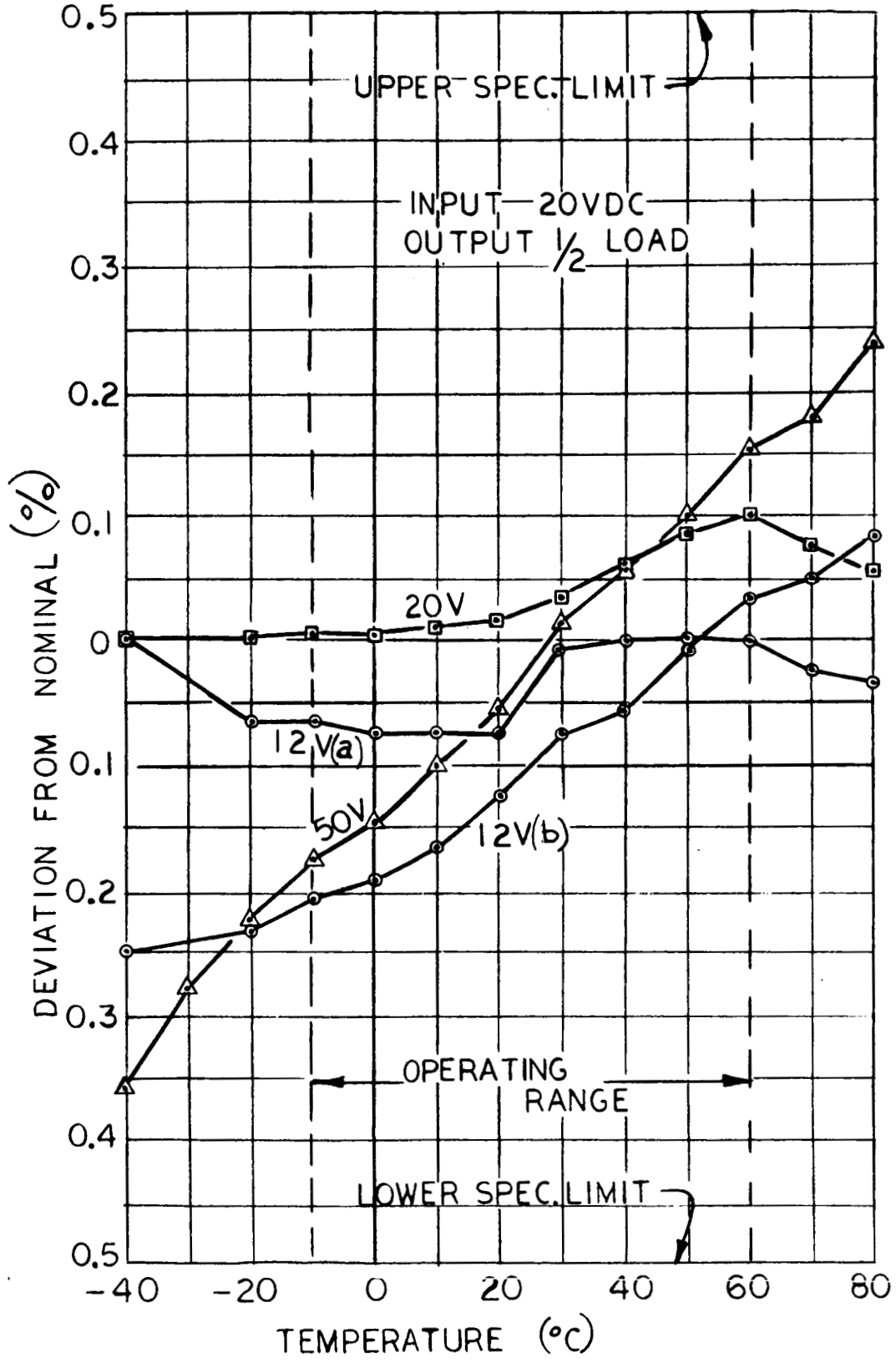


FIGURE 22. VOLTAGE VS TEMPERATURE.

CONVERTER OUTPUT	SPECIFIED LIMITS (VDC)		MEASURED VOLTAGE (VDC)	CONDITIONS		
				INPUT (VDC)	LOAD (I)	TEMP (C^{o})
12 (a)	MAX	12.06	12.00	20	MIN	+60
	MIN	11.94	11.98	12	FULL	-10
12 (b)	MAX	12.06	12.01	20	MIN	+60
	MIN	11.94	11.97	12	FULL	-10
20	MAX	20.10	20.03	20	MIN	+60
	MIN	19.90	19.98	12	FULL	-10
50	MAX	50.25	50.10	20	MIN	+60
	MIN	49.75	49.86	12	FULL	-10

TABLE IV. WORST CASE OUTPUT VOLTAGE.

2. Dynamic Regulation

When the unit is subjected to a step change in input voltage (10 millisecond rise time) between the limits of 12V and 20V, the output voltages change only slightly. Maximum excursions from the output voltages prior to the input voltage step change are summarized in Table V.

TABLE V. DYNAMIC REGULATION FOR INPUT VOLTAGE CHANGE (12V-20V, 10ms).

CONVERTER OUTPUT		12V(a)	12V(b)	20V	50V
MAXIMUM EXCURSION (MV)	OBSERVED	<10	<10	15	60
	SPECIFIED	60	60	100	250

Dynamic regulation for step changes in load current is required only on the 12V outputs with no specified rise time. A mercury relay was used to provide an essentially instantaneous load change. The output capacitors for the 12V free running switching-mode regulators were chosen to meet the dynamic regulation requirement of ± 1/2 percent excursion. A less stringent requirement (i.e. a larger excursion or longer rise time) could be met with fewer output capacitors. Test results under worst-case conditions are shown in Figure 23 (12V(b) output shifted between 50 mA and 1000 mA, other outputs at full load, input voltage to unit at 12VDC). The maximum excursion was 50mV.

B. Output Ripple and Noise

Output ripple is well within specification under all specified conditions. Worst case conditions occur at high temperature (where storage time is greatest) and at minimum load (where damping is least). The ripple increases for both low and high extremes of input voltage (see Figure 5), but is greatest at the lowest input. The ripple performance is summarized in Table VI.

TABLE VI. OUTPUT RIPPLE.

CONVERTER OUTPUT	PEAK-TO-PEAK OUTPUT RIPPLE (mV)		
	SPEC. MAX.	WORST CASE ($12V_{IN}$, 60°C, MIN LOAD)	TYPICAL ($20V_{IN}$, 25°C, 1/2 LOAD
12 (a)	10	5	5
12 (b)	10	5	5
20	10	5	2
50	20	10	3

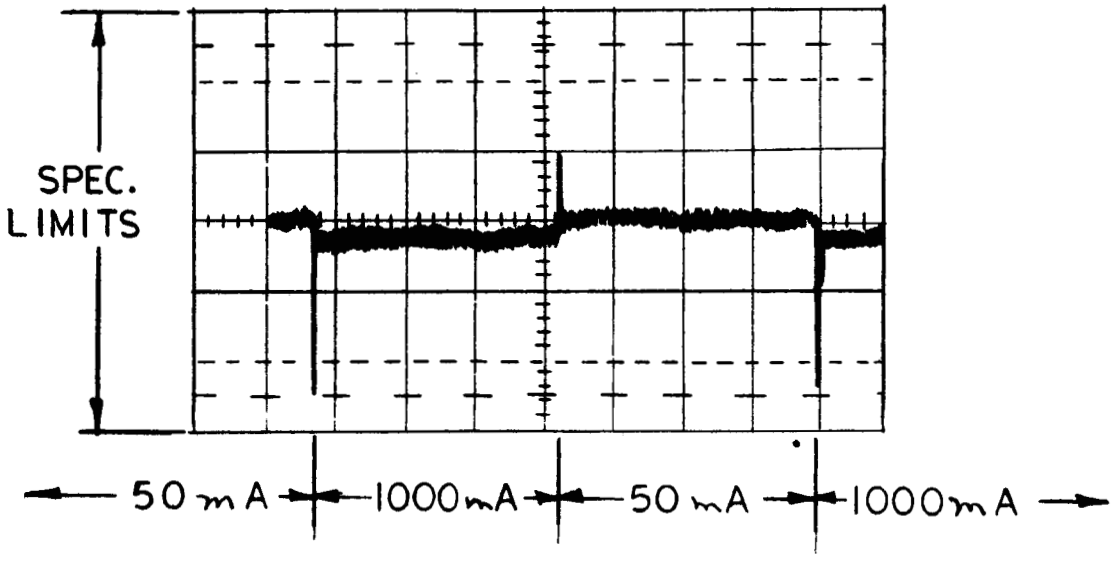


FIGURE 23. DYNAMIC REGULATIONS FOR LOAD CHANGE, 12V(b) OUTPUT.

[VERTICAL 20 mV/DIV
HORIZONTAL 5 mSEC/DIV]

In addition to the ripple (which occurs at the 7 to 10 KHz frequency of the free running switching-mode regulators) there is an unclassified noise in the form of spikes. The amount of noise measured depends critically on the measuring technique since there is no RFI filtering or shielding on the breadboard. A packaged converter with the usual RFI filters and shields would meet the specified 50mV (100mV on the 50V output) peak-to-peak noise requirement.

C. Efficiency

Efficiency of the EMCR131A is well above the required 85% at full load and reaches the maximum efficiency of 88.4% at high input voltage, as shown in Figure 24. As the load power is reduced, efficiency decreases slightly, but is still above 85% at half load. As lighter loads are approached, however, the fixed losses of the redundant circuitry become more apparent and efficiency decreases, see Figure 25. At minimum load, efficiency is below the required 80% but reaches 80% at loads only slightly greater than minimum. Efficiency varies only slightly over the entire temperature range. Figure 26 shows the actual power loss under various conditions and Figure 27 is a breakdown of this power loss under typical conditions (20V input, 1/2 load).

D. Output Protection

All four free running switching-mode regulator output are current limited at a minimum 150% of normal load. The current limiting circuit is redundant and designed to insure against loss of output voltage except under a valid overload. As shown in Figure 12 output voltage drops sharply at

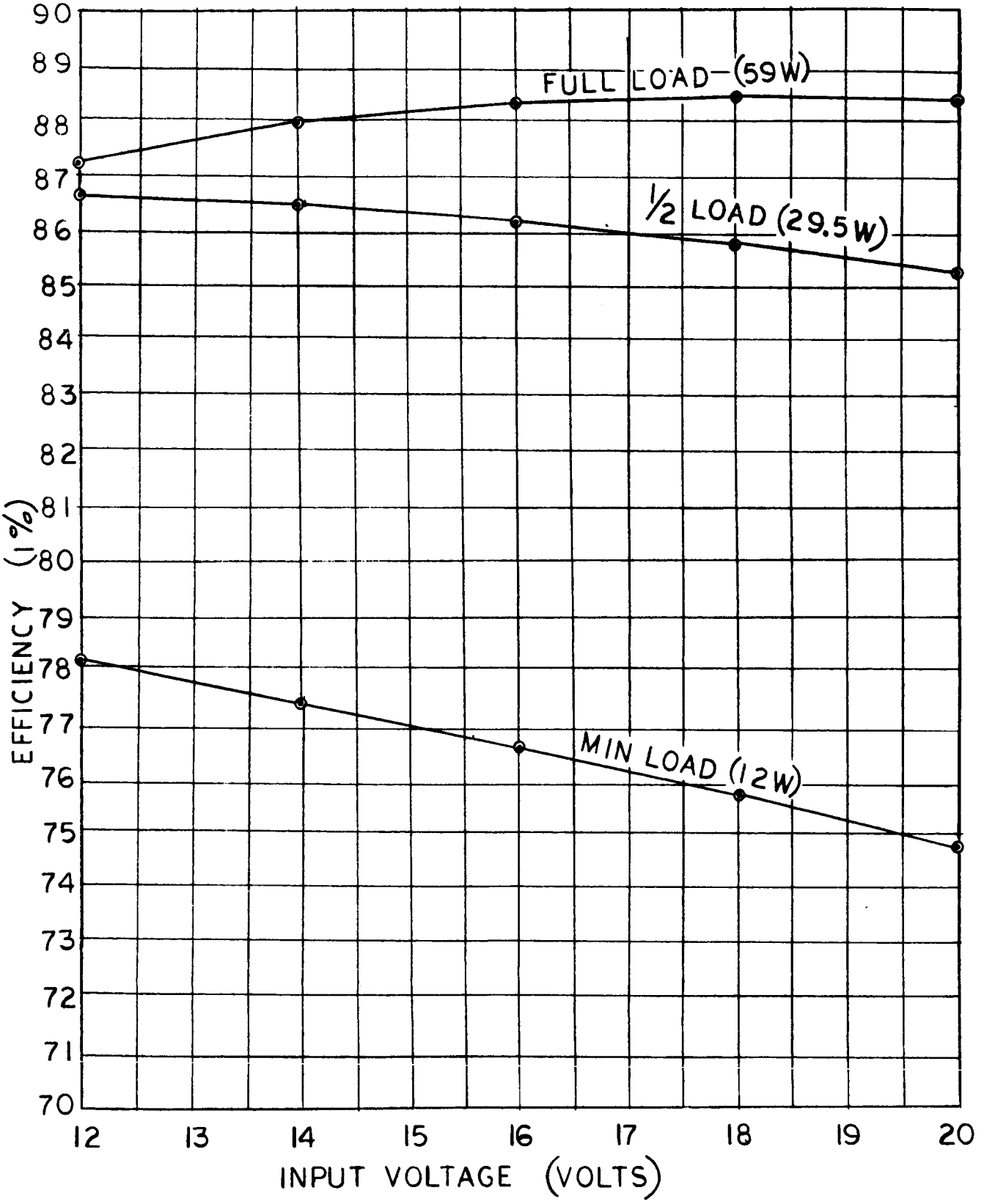


FIGURE 24. EFFICIENCY VS INPUT VOLTAGE.

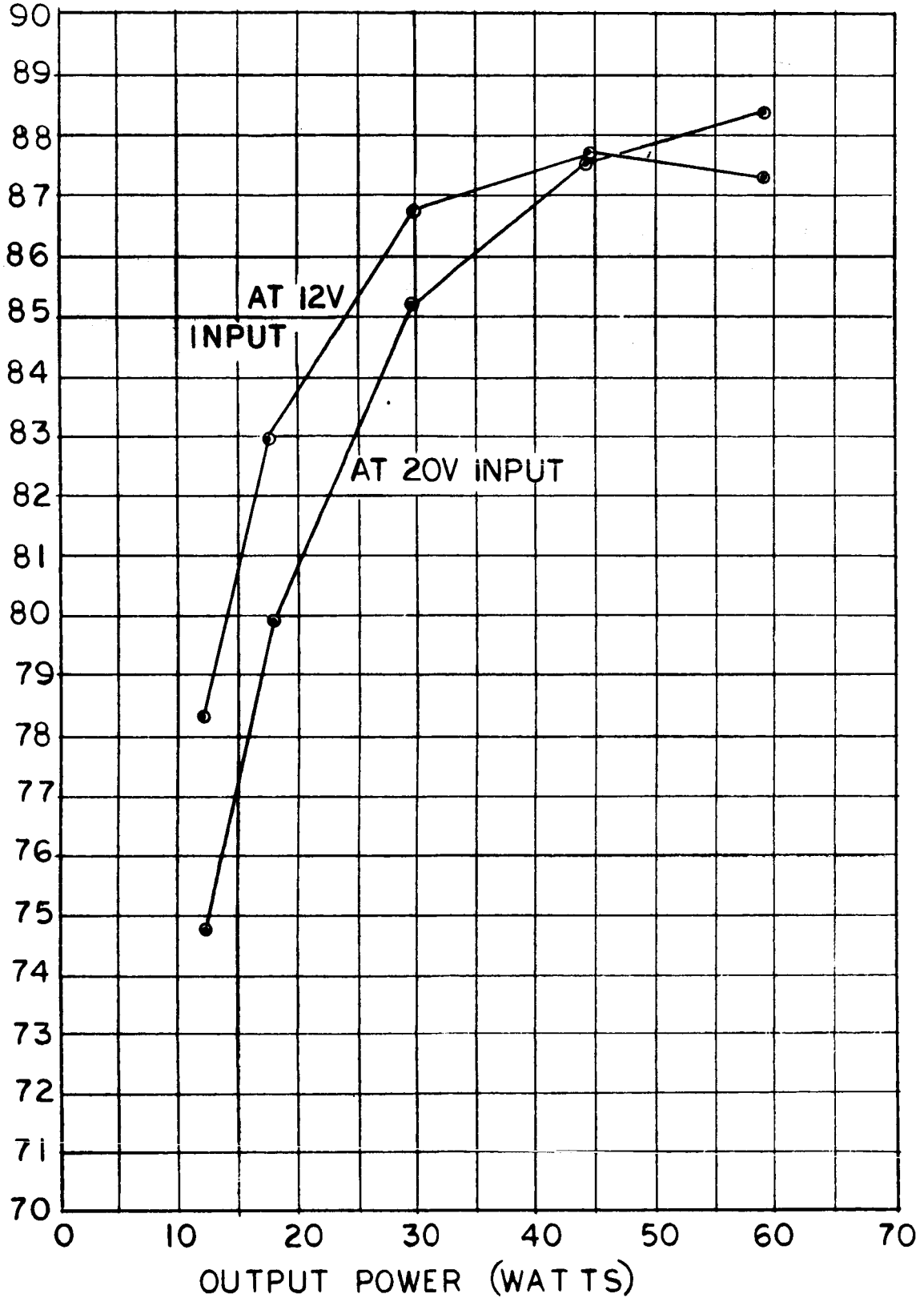


FIGURE 25. EFFICIENCY VS OUTPUT POWER.

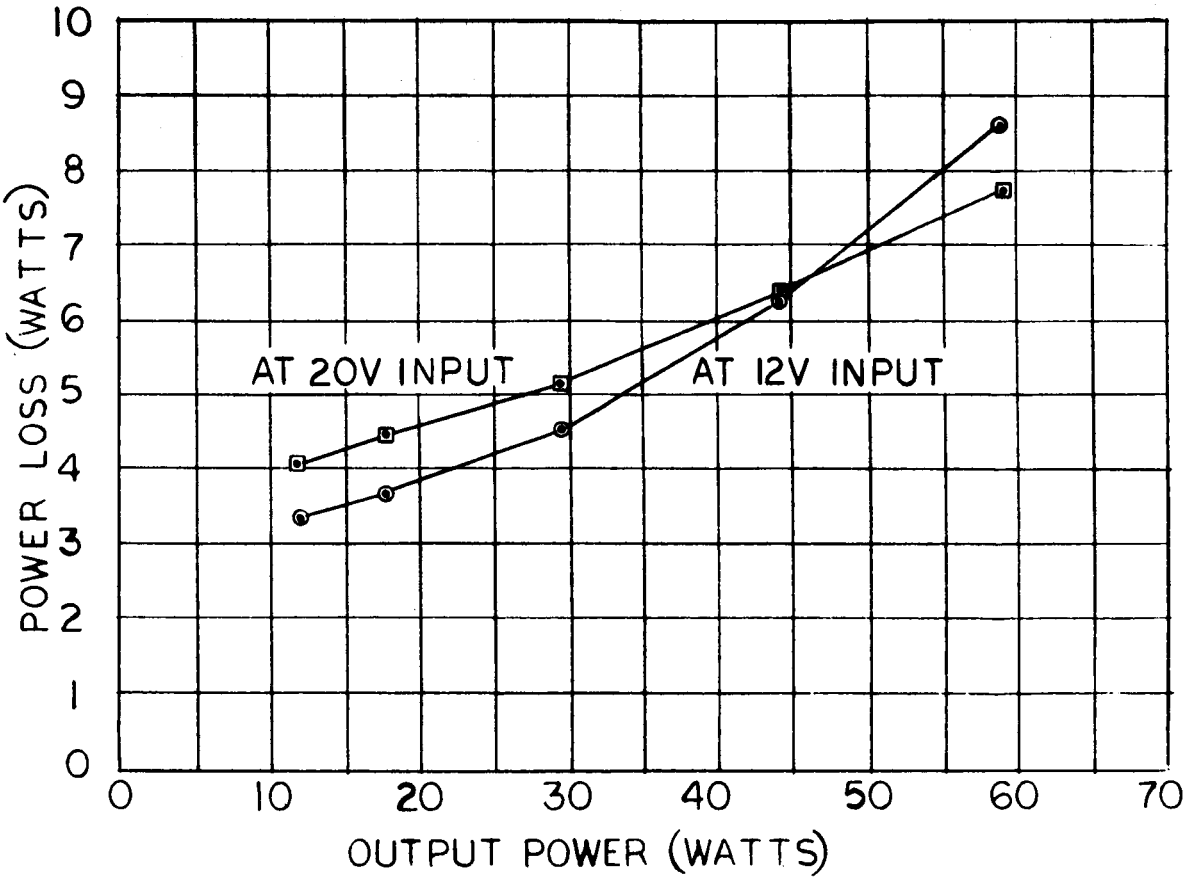
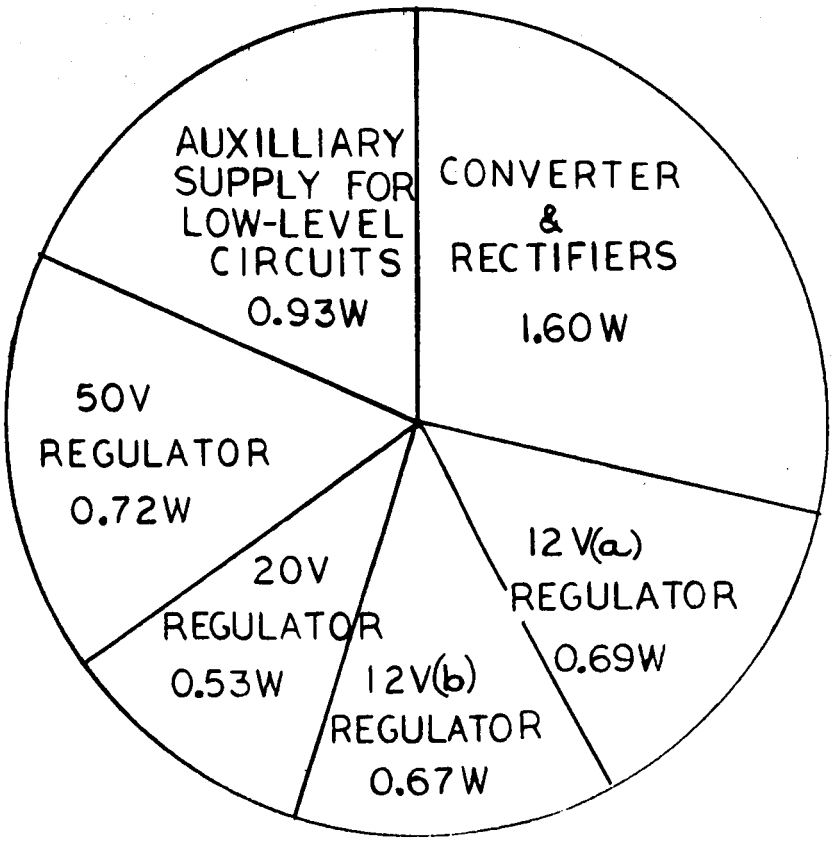


FIGURE 26. POWER LOSS VS OUTPUT POWER.



TOTAL LOSS= 5.14W

FIGURE 27. POWER LOSSES.
(20V INPUT, 1/2 LOAD)

some current slightly greater than 150% of normal load. As the load resistance is decreased to a short circuit, the current increases only a few percent. The free running switching-mode regulator output currents are shown in Figure 28 as functions of temperature. Two overload conditions are illustrated: 200% load* which gives a current near the break point of the voltage current plot, and a dead short which gives the maximum current obtainable. The data plotted on Figure 28 is at 20V input but the variation with input voltage is small.

E. Input Noise, RFI, Size and Weight.

The converter is required to contribute no more than 20MV peak-to-peak noise back into an input with 0.1 ohm to 1.0 ohm impedance. The EMCR131A meets this unusually severe restriction under all conditions (worst case is 15MV peak-to-peak at 60°C, 12V input, full load) but the input filter required weights more than 9 oz. A survey of sattelite power supplies in this power range reveals that requirements are typically 100MA to 200MA peak-to-peak noise current. These less severe specifications can be met with much lighter filters.

The breadboard contains no RFI filtering or shielding. A flight unit would, of course, include these components and would contribute negligible electromagnetic interference to the environment of the unit within the spacecraft. The electromagnetic interference specification for this unit is MIL-I-6181B which requires the ability to accept a 3 volt RMS audio input on the power input lines without affecting the output significantly. Such

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* This is 200% of normal full load conductance. Load resistance is half of normal full load resistance.

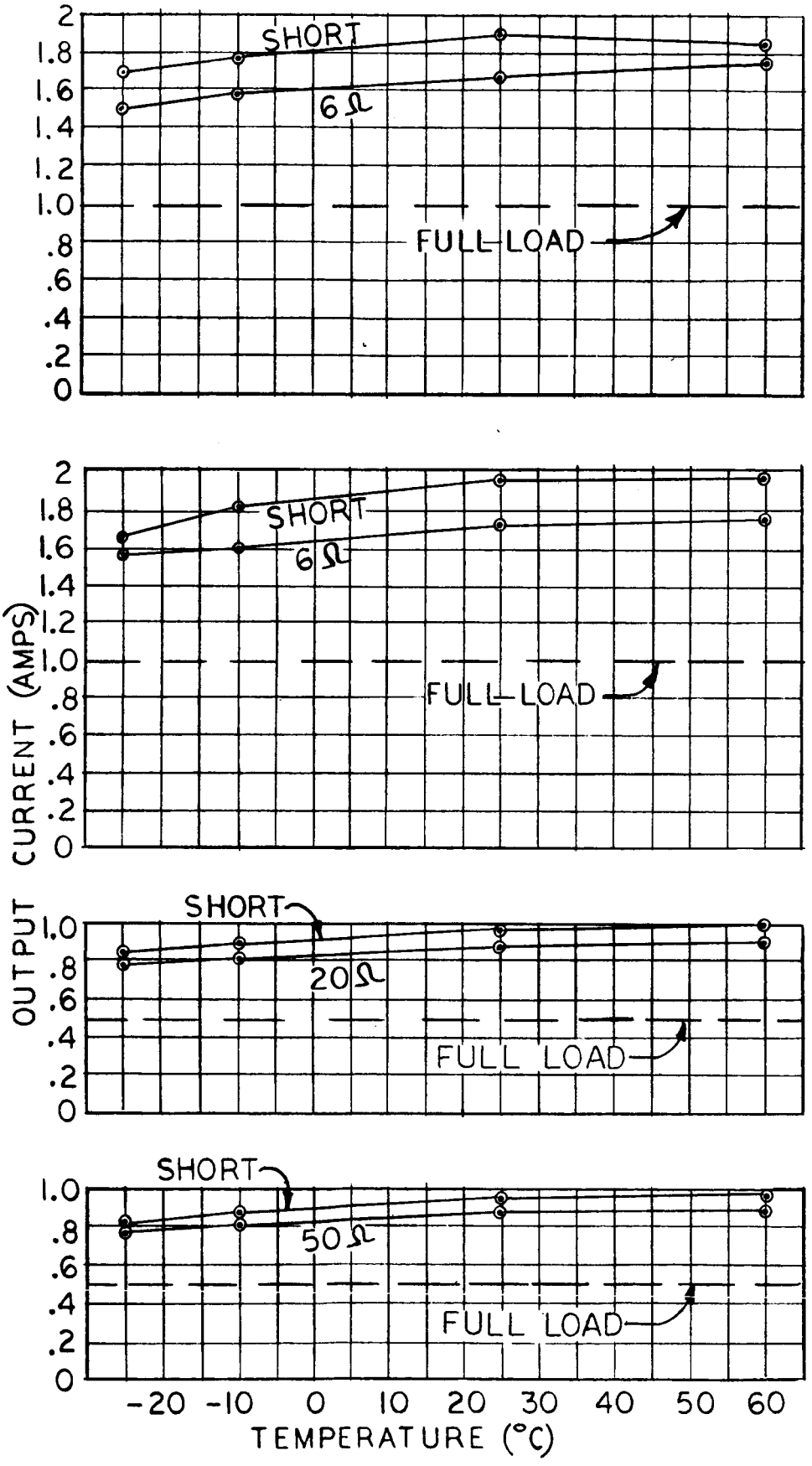


FIGURE 28. OUTPUT CURRENT (OVERLOAD) VS TEMPERATURE.

an input is rarely encountered in a sattelite power system. The requirement is usually waived or modified, because to meet it at low input voltage means a larger transformer ratio and a lower efficiency.

The component parts for the converter weight 3.3 pounds, including the input filter - slightly larger than the design goal of 3.0 pounds. It might be possible (by the use of welded modules) to fit these component parts into a 9 X 5 X 2 inch box as specified, but this depends on the type of mounting, connector, and size of RFI filtering. A slightly larger size would give much greater design freedom and accessibility.

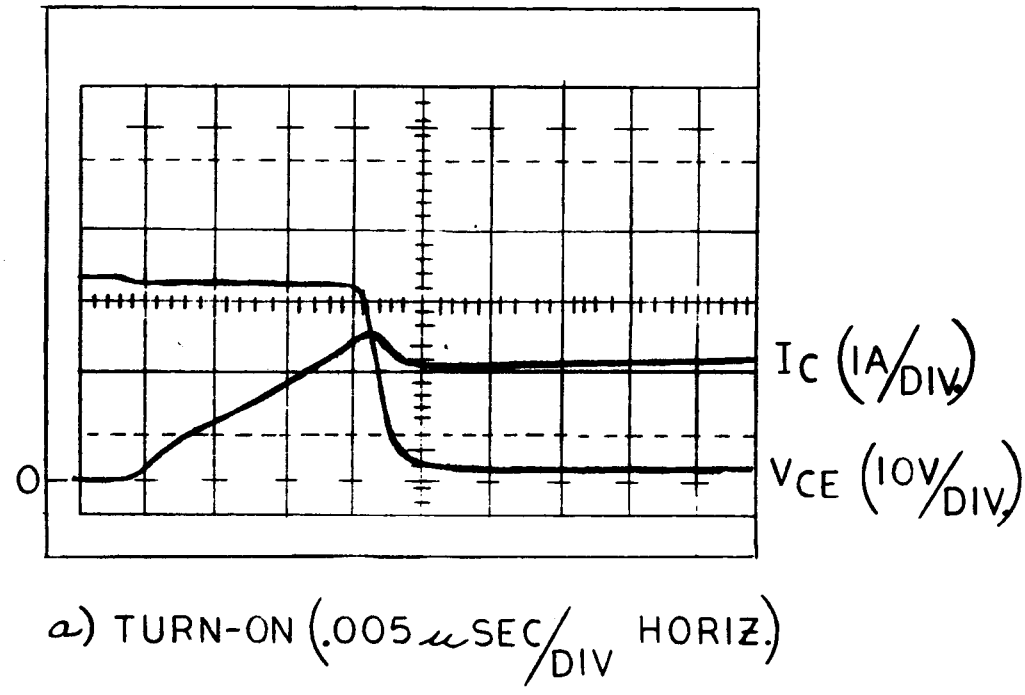
V. RELIABILITY

A. Stress Levels

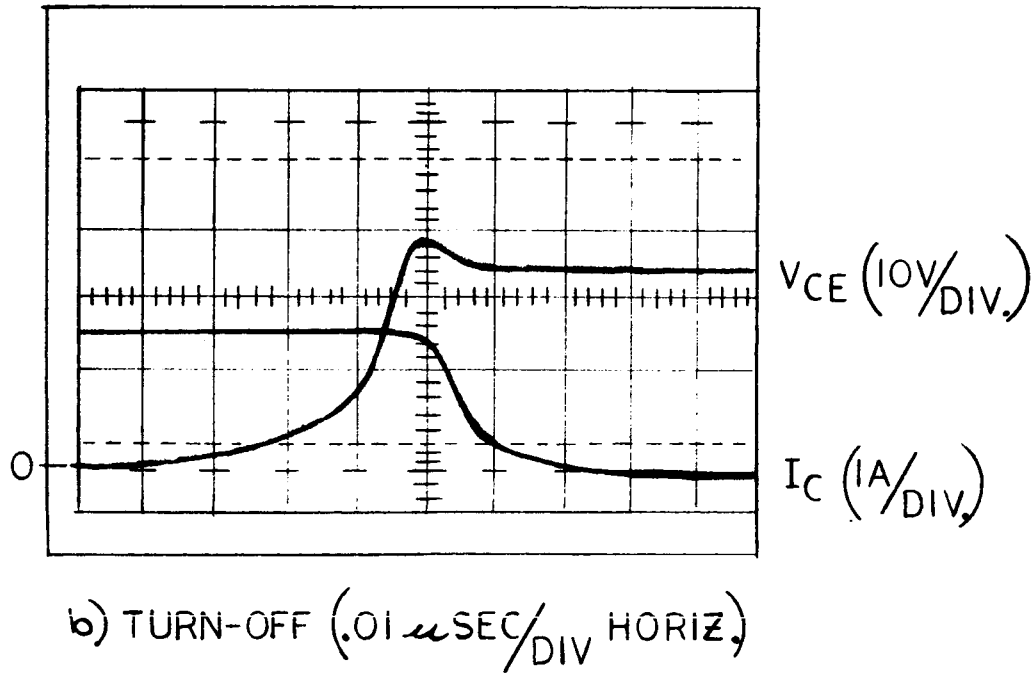
All component parts of the EMCR131A are operated well within their specified ratings. For most components, the maximum stress levels reached may be easily determined from the circuit applications of the component parts and a few calculations. Peak stresses on the power transistors are more difficult to calculate, however, since there peaks occur during rapid switching between the "off" state and the saturated "on" state. To verify that the power transistors were operating safely, collector current and collector-emitter voltage were obtained simultaneously on an oscilloscope. Photographs showing the short turn-on and turn-off periods were taken of the oscilloscope screen for worst-case conditions of input voltage and load. The photographs (such as those shown in Figure 29) were then used to plot collector current vs collector-emitter voltage. These current-voltage switching curves could then be compared to the manufacturers safe operating area specifications for the power transistors. Switching curves are shown in Figure 30 for the four types of power transistors. Safe operating areas are shown for the shortest time periods specified by the manufacturers, although switching is actually completed in a fraction of a microsecond. The graph of Figure 30b corresponds to the photograph of Figure 29.

B. Calculated Reliability

An estimate of the reliability of the EMCR131A may be calculated using the extensive test data available for high-reliability component parts. Each component part is assigned a failure rate, λ, (failures/hr) based on this test data. For the high reliability component parts used in this unit, the failure rates are very small - on the order of 10^{-8} failures/hr - and occur at random.

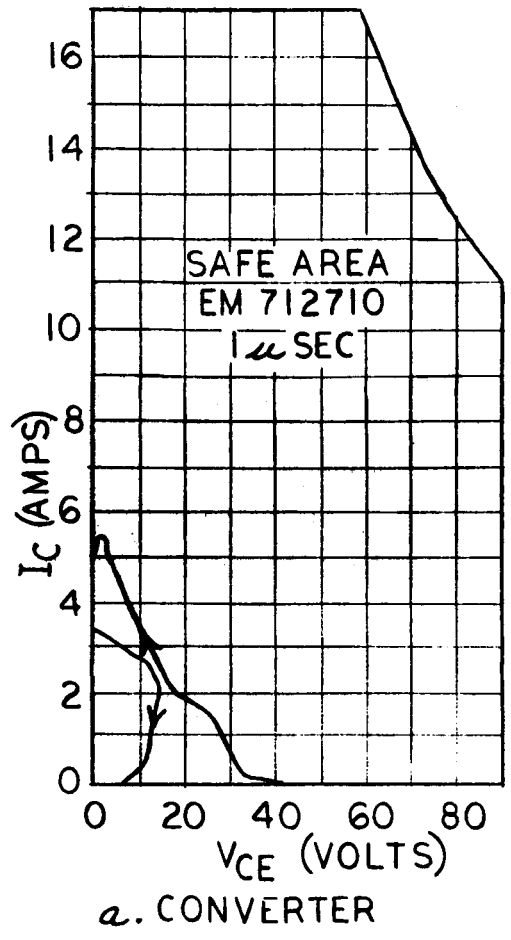


a) TURN-ON (.005 μSEC/DIV HORIZ.)

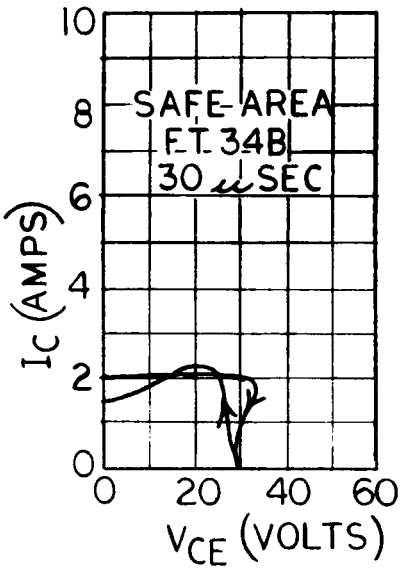


b) TURN-OFF (.01 μSEC/DIV HORIZ.)

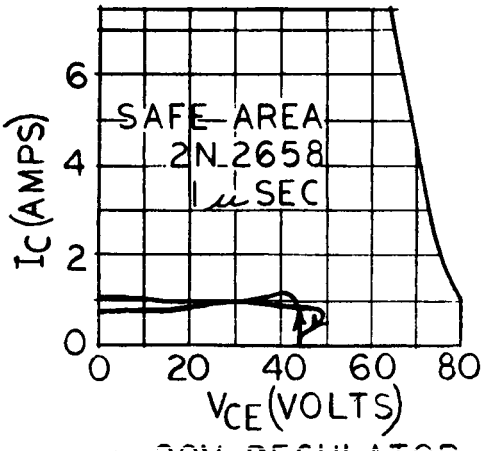
FIGURE 29. POWER TRANSISTOR (12V REGULATOR) CURRENT & SWITCHING.
(INPUT=20VDC, LOAD=SHORT)



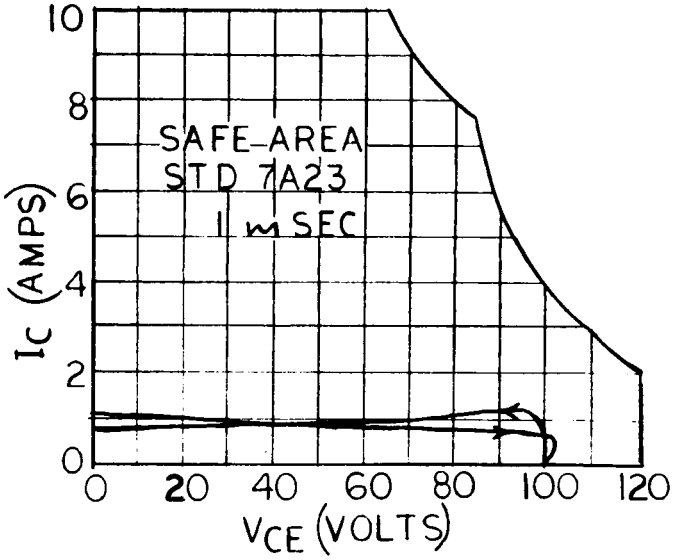
a. CONVERTER



b. 12V REGULATOR



c. 20V REGULATOR



d. 50V REGULATOR

FIGURE 30. WORST CASE SWITCHING CURVES OF POWER TRANSISTORS INPUT 20VDC, a. FULL LOAD, b, c, d SHORTED LOAD.

The reliability, R, is defined as the probability that the unit will survive for the duration, t, of the mission. For non-redundant circuits, it is assumed that a failure of any component part constitutes a failure of the unit. The reliability is given by,

$$R = e^{-t\sum\lambda}$$

where $\sum\lambda$ is the sum of the failure rates of all components in the unit.

If the unit had been designed on the basis of one converter followed by four non-redundant free running switching-mode regulators, the reliability could have been calculated by summing all the λ's for one converter and four regulators.

$$\sum\lambda \text{ (conv)} = 79.2 \times 10^{-8} \text{ failures/hr}$$
$$\sum\lambda \text{ (reg.)} = 650 \times 10^{-8} \text{ failures/hr}$$
$$\sum\lambda \text{ (total)} = 2679.2 \times 10^{-8} \text{ failures/hr}$$

For the required 30,000 hour mission,

$$R \text{ (total)} = e^{-30{,}000 \times 2680 \times 10^{-8}} = 0.447$$

Alternately, the reliability of each section could be calculated separately, and the overall reliability obtained by multiplying

$$R \text{ (conv)} = e^{-30{,}000 \times 79.2 \times 10^{-8}} = 0.97651$$
$$R \text{ (reg)} = e^{-30{,}000 \times 650 \times 10^{-8}} = 0.82300$$
$$R \text{ (total)} = R(\text{conv}) \times R(\text{reg}) \times R(\text{reg}) \times R(\text{reg}) \times R(\text{reg})$$
$$= 0.447$$

as before. This low figure, less than 50% chance of success, was not acceptable, so some form of redundancy was clearly necessary.

The simple but brutal technique of putting two complete DC/DC Converters in parallel, or using parallel power stages in each free running switching-mode regulator, has several serious disadvantages:

a. Considerable increase in weight. The size and weight of the chokes is largely determined by the current that causes them to saturate. Thus the total choke weight of both supplies would be twice the choke weight of one supply of the present design. The total weight of both power transformers, however, might be made about the same as that of a single one of present design (although this would mean degraded efficiency if one supply should fail).

b. Increased power loss. Since the free running switching-mode regulators are not current driven, each must be designed to carry the full load current. The bases of the power transistors must be driven accordingly, which takes twice as much drive power as for a single unit. In addition, this harder drive would increase the switching storage time of the power transistors under normal operation and therefore heavier filters would be required.

c. In order to remove a supply from the system, fuses (with accurate ratings) would be required and the current limiting incorporated in the DC/DC Converter would make it difficult to blow these fuses.

The very low ripple requirements make high gain wideband circuits containing many component parts necessary. Fortunately, most of these component parts operate at low levels and are compatible with intergrated circuits. The redundant voltage sense modules and current limiting circuits include most of these low level component parts.

The reliability of redundant circuits is enormously better than for non-redundant circuits with similar numbers of parts. Calculation for redundant circuits are easily accomplished using the unreliability, Q, which is the probability of failure.

$$Q = 1-R$$

A reliability block diagram of the 12V free running switching-mode regulator is shown in Figure 31. Since the voltage sense circuits operate on a majority basis, two must fail in order for the signal to the driver to be incorrect. This might happen in any of four ways:

Condition	Probability
W1 and W2 fail	$Q_1 \times Q_2 = Q_1^2$
W2 and W3 fail	$Q_2 \times Q_3 = Q_1^2$
W1 and W3 fail	$Q_1 \times Q_3 = Q_1^2$
W1 and W2 and W3 fail	$Q_1 \times Q_2 \times Q_3 = Q_1^3$

The probability that any of these conditions will exist is then

$$Q_w = 3Q_1^2 + Q_1^3$$

The failure rate for each voltage sense module is $\lambda = 116.5 \times 10^{-8}$ filters/hr.

Therefore,

$$Q_1 = 1-R, = 1-e^{-30,000 \times 116.5 \times 10^{-8}} = .0349$$

$$Q_w = .00370$$

$$R_w = 1-Q_w = .99630$$

which is a substantial improvement oyer a single non-redundant voltage sense module. Actually it is likely that if two voltage sense module failed in opposite directions (i.e. W1 "on" and W2 "off") the remaining voltage sense module would still control the free running switching-mode regulator and no overall failure would occur. The estimate above is therefore conservative.

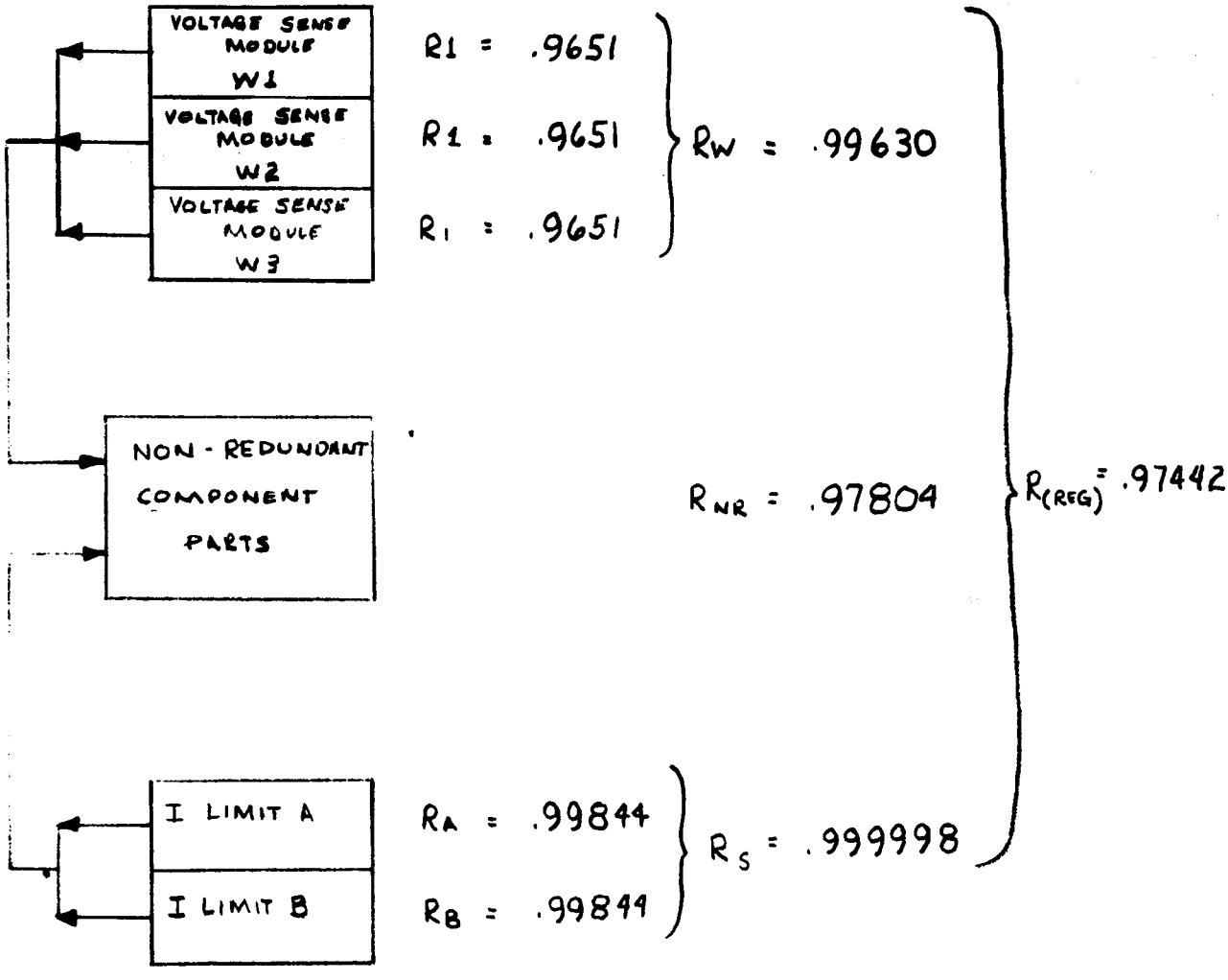


FIGURE 31. RELIABILITY BLOCK DIAGRAM, 12V FREE RUNNING SWITCHING-MODE REGULATOR.

The current limiting circuits present a different type of redundancy. Here, only those conditions which lead to a premature shut-down of one output need be considered as a failure. Referring to the schematic, Figure 11, the failure rate for section A is $\lambda_A = 15.5 \times 10^{-8}$ failure/hr. However, only 5.18×10^{-8} of these would turn transistor Q51 on - the others would turn it off. Both Q51 and Q52 must turn on prematurely for a failure to occur. The probability that this will happen is

$$Q_s = Q_A Q_B \cong Q_A^2 = (1 - e^{-30{,}000 \times 5.18 \times 10^{-8}})^2$$

$$= 0.00000243$$

$$R_s = 0.99999757$$

The rest of the free running switching-mode regulator is non-redundant and the failure rates of these non-redundant component parts sum to $\lambda_{NR} = 74.1 \times 10^{-8}$ failures/hr of which almost half would occur in the output capacitor bank.

Therefore

$$R_{NR} = e^{-30{,}000 \times 74.1 \times 10^{-8}} = .97804$$

The reliability of the free running switching-mode regulator is thus $R(12V\ reg) = R_w \times R_s \times R_{NR} = .97442$

The reliability of the 20V and 50V free running switching-mode regulators are calculated in a similar way and the results are

$R(20V\ reg) = .98661$

$R(50V\ reg) = .98595$

which are higher because there is no load transient requirement on these outputs, therefore fewer capacitors are required.

Although these redundant circuits improved the free running switching-mode regulator reliability greatly, they required an auxilliary power supply. As described in Section III paragraph D, Power for Low Level Modules, this auxilliary power supply is

fully redundant itself. Each section contains a switching regulator ($\lambda = 32.3 \times 10^{-8}$ failures/hr) and a converter ($\lambda = 43.8 \times 10^{-8}$ failures/hr). Each section then has

$$Q_A = Q_B = 1 - e^{-30,000 \times 76.1 \times 10^{-8}} = .0226$$

and since both sections must fail in order to cause an overall failure,

$$Q(aux) = Q_A^2 = .000511$$

$$R(aux) = 1-Q = .999489$$

The reliability of the entire unit is the product of these separate figures.

$$R(tot) = R(conv) \times R(12V\ reg)^2 \times R(20V\ reg) \times R(50V\ reg) \times R(aux)$$

$$= (.97651) \times (.97442)^2 \times (.98661) \times (.98595) \times (.00049)$$

$$= .90146$$

This figure indicates more than 90% probability of completing a mission of nearly four years in a space environment with no failures and negligible drift.

APPENDIX

FREE RUNNING SWITCHING-MODE REGULATORS

FREE-RUNNING SWITCHING-MODE REGULATORS

A. Analysis

The basic free-running switching-mode regulator is shown in Figure 1. This free-running switching-mode regulator converts an unregulated DC input voltage, E_1, to a lower

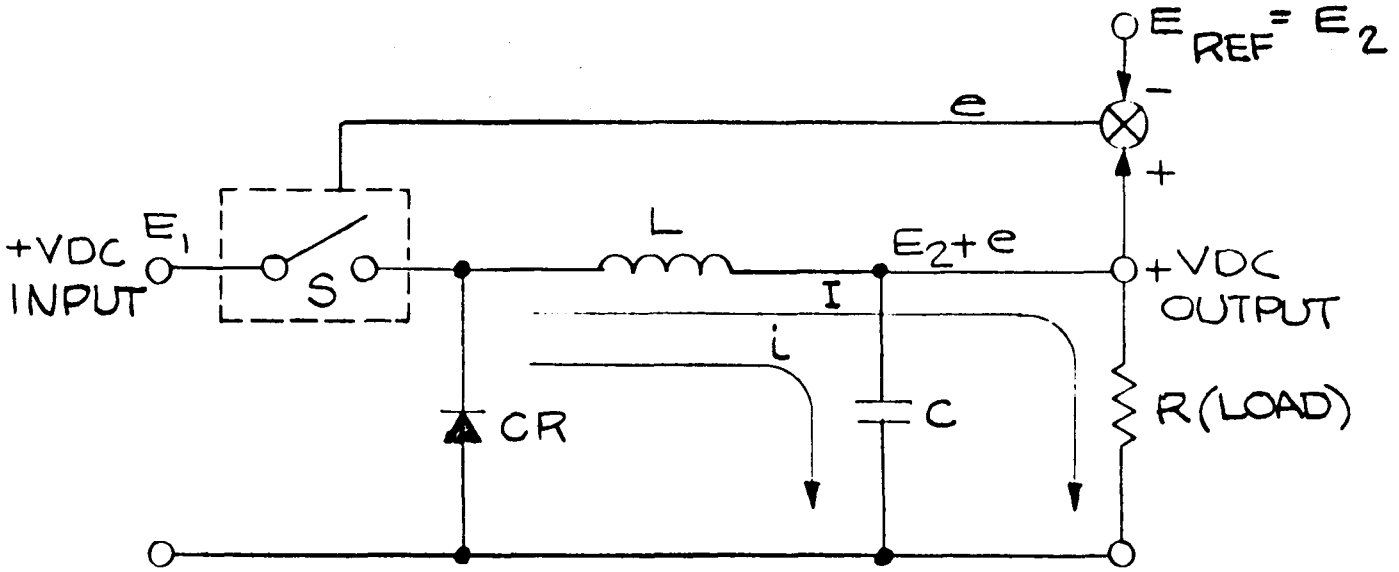


FIGURE 1. FREE-RUNNING SWITCHING-MODE REGULATOR IDEAL CIRCUIT.

and regulated DC output voltage, E_2, by alternately opening and closing the switch, S, at a high repetition rate.

A small ripple voltage, e, varying at the switching rate, appears superimposed upon E_2. E_2 + e is compared to a reference voltage, E_{ref}, equal to the desired E_2, by means of a comparator with hysteresis d. Thus when e increases to $+\frac{d}{2}$ the switch S opens causing the choke voltage to reverse to the point where CR conducts. When e decreases to $-\frac{d}{2}$, S closes again. Since the switching frequency is high (perhaps 10 kHz), RC is large (>10 ms), and e is small (<10 mv); the voltage across L is approxi-

mately E_1-E_2 when S is closed and approximately $-E_2$ when S is open. Thus a nearly constant current (I) flows in the load, a triangular current (i) flows in L and C, and both currents (I + i) flow in the inductor L. The voltage and current waveforms are shown for d = 0 in Figure 2.

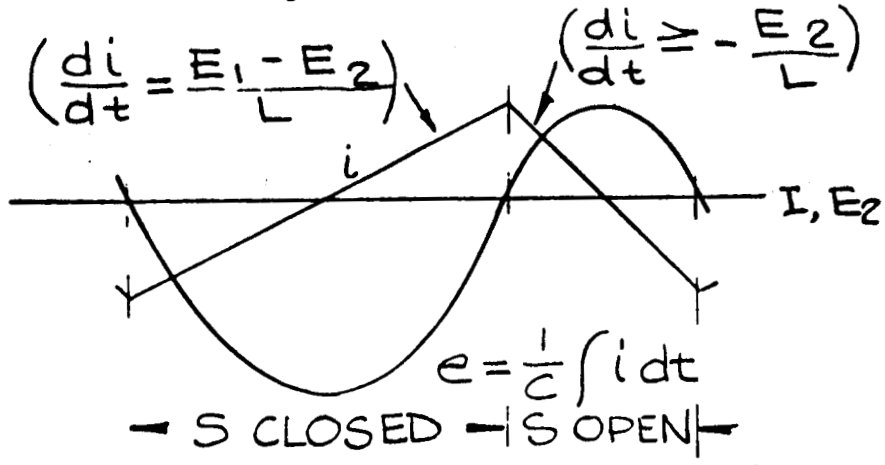


FIGURE 2. CURRENT AND VOLTAGE, IDEAL CIRCUIT.

Figure 2 shows several interesting features. The output ripple voltage is 90° out of phase with the circulating current and is composed of parabolas whose amplitudes depend upon the DC voltages. Note that e may contain a DC component. Note also that nothing determines the operating frequency except the initial conditions-the waveforms could just as well have been drawn for a lower frequency, higher peak-to-peak current, and higher ripple. This is the first clue that the model of Figure 1, with ideal components, is not an adequate description of a working regulator. If the hysteresis is not zero, the amplitude of e and of i will increase with each cycle until the losses damp it out (or until $\frac{i}{2}$ is greater than I, where the reverse currents change the mode of operation.)

Since

$$e = \frac{1}{c}\int i\ dt \qquad (1)$$

and if e is to increase by an amount d during the time S is closed, then i must not be symmetrical about zero - it must have a net increase in amplitude. There will be another net increase in amplitude while the switch S is open, and so on. This is shown in Figure 3.

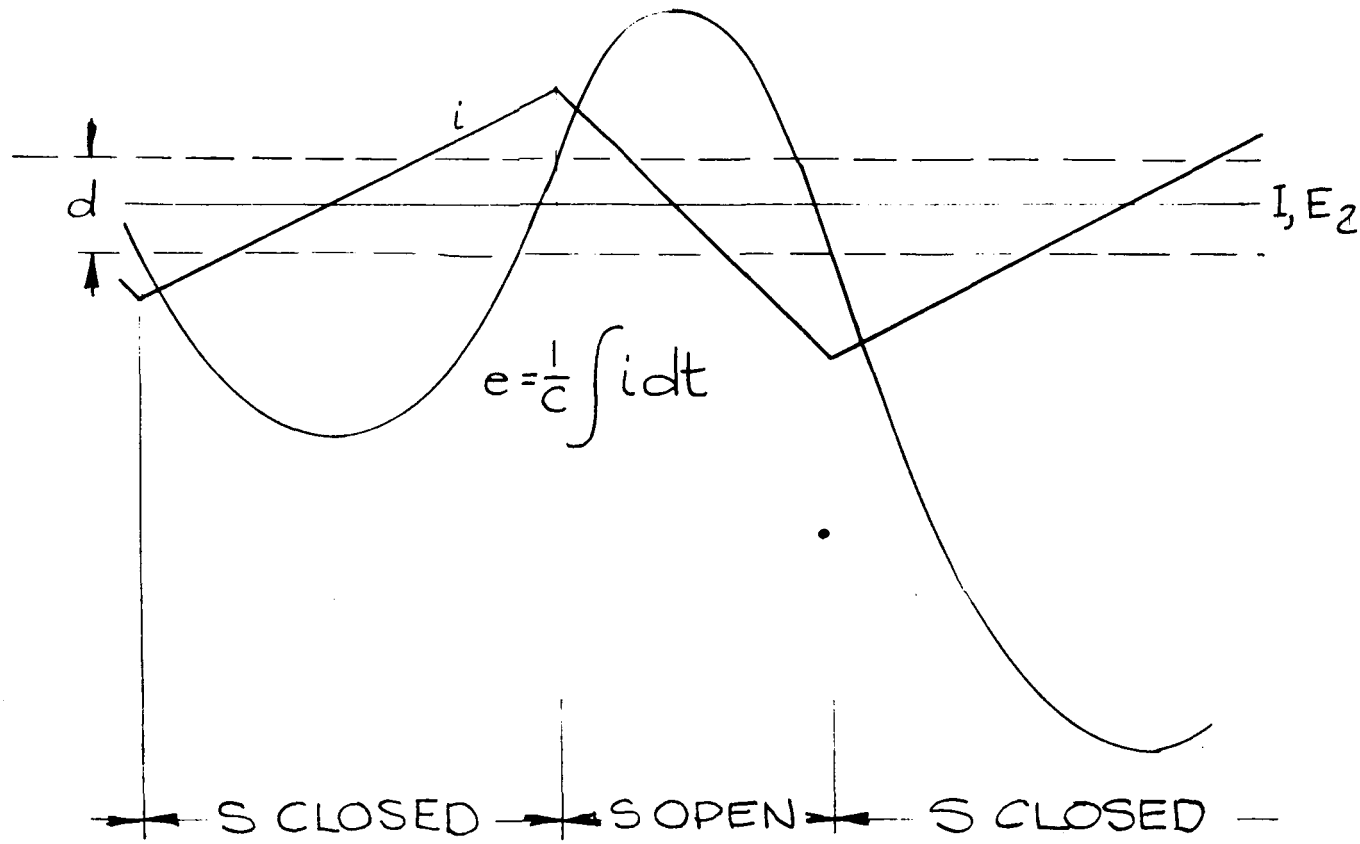


FIGURE 3. IDEAL CIRCUIT WITH HYSTERISIS UNSTABLE.

Any time delay in the feedback loop, such as storage time of a power transistor used as the switch S, will cause a similar instability.

Actually, the regulator circuit shown in Figure 1 does work in practice (the EMCR131 used four of these regulator circuits quite successfully) so there must be some losses or feedback phase leads in the actual circuit which were not included in our ideal model. Observation of the actual e waveform indicates that the series resistance, R_c, within C is responsible for the stability. To demonstrate how this occurs, we shall develop an expression for the current and, from this, derive an expression for the ripple voltage in terms of the circuit parameters.

The circuit diagram in Figure 4 is a much more accurate representation of an actual free-running switching-mode regulator than the one shown in Figure 1. This circuit produces the waveforms shown in Figure 5.

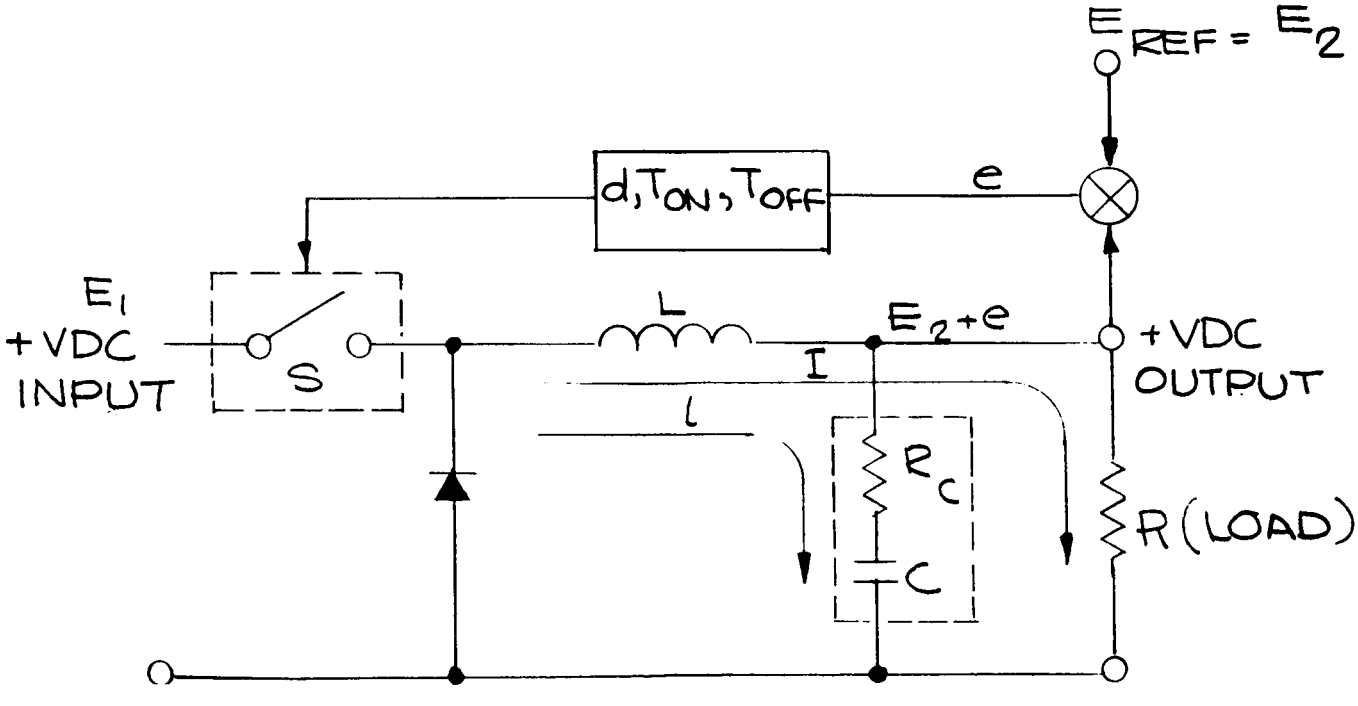


FIGURE 4. FREE-RUNNING SWITCHING-MODE REGULATOR, NON-IDEAL CIRCUIT.

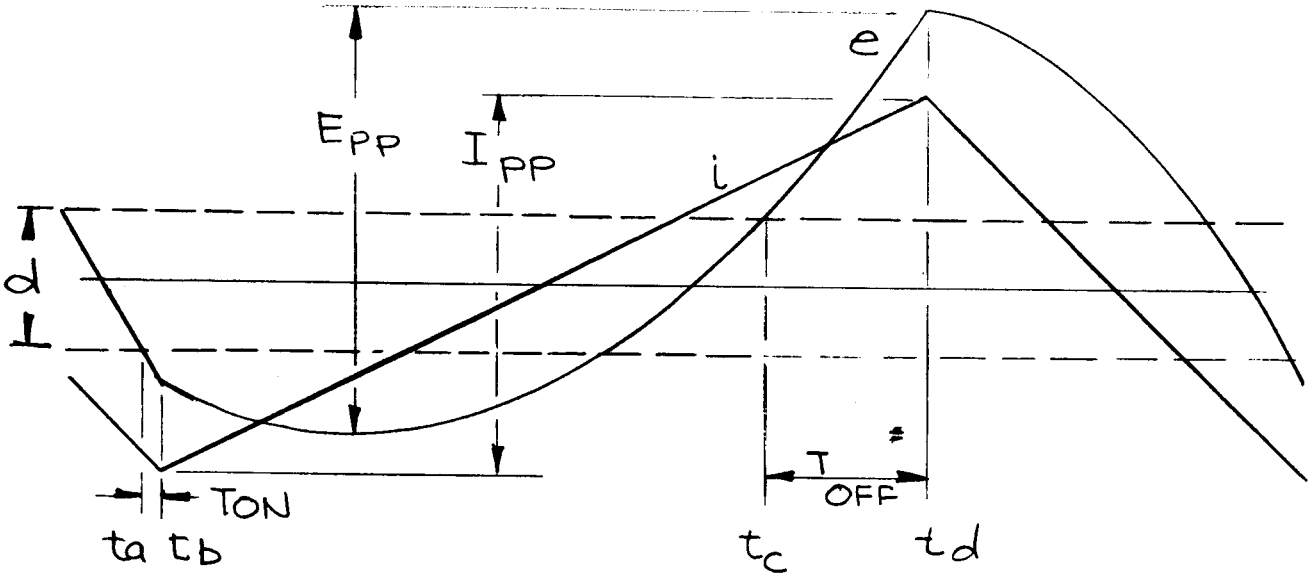


FIGURE 5. CURRENT AND VOLTAGE ACTUAL CIRCUIT.

At some point, t_a, during the cycle, e will be decreasing and will pass through $-\frac{d}{2}$. Since the feedback loop contains a number of transistors, the main switching transistor does not turn on until a short time delay, T_{on}, has elapsed. This brings us to time t_b (see Figure 5), at which time

$$e_b = e_a + (i_b - i_a)R_c + \frac{1}{C}\int_{t_a}^{t_b} i\,dt \qquad (2)$$

Between t_a and t_b the current is

$$i = -\frac{I_{pp}}{2} + \frac{E_2}{L}(t_b - t) \qquad (3)$$

where I_{pp} is the peak-to-peak amplitude of the triangle current and is the dependent variable to find. By combining equations 3 and 2 and integrating,

$$e_b = -\frac{d}{2} - \frac{E2}{L} T_{on}R_c - \frac{I_{pp}}{2C} T_{on} + \frac{E_2}{2LC} T_{on}^2 \qquad (4)$$

During the time the switch S is closed (between t_b and t_d), the current and voltage are

$$i = \frac{-Ipp}{2} + \frac{E_1 - E_2}{L}(t-t_b) \tag{5}$$

$$e = e_b + (i-i_b)\,R_c + \frac{1}{c}\int_{t_b}^{t} i\,dt \tag{6}$$

By combining equations 5 and 6 and integrating,

$$e = e_b + \frac{E_1 - E_2}{L}(t-t_b)\,R_c - \frac{Ipp}{2c}(t-t_b) + \frac{E_1 - E_2}{2LC}(t-t_b)^2 \tag{7}$$

Evaluating this at time t_c, when the voltage has increased to $+\frac{d}{2}$ and by using equation 4,

$$e_c = \frac{d}{2} = -\frac{d}{2} - \frac{E_2}{L}T_{on}R_c - \frac{I_{pp}}{2c}T_{on} + \frac{E_2}{2LC}T_{on}^2 + \frac{E_1 - E_2}{L}(t_c-t_b)R_c - \frac{I_{pp}}{2c}(t_c-t_b) + \frac{E_1 - E_2}{2LC}(t_c-t_b)^2 \tag{8}$$

Although e has reached $\frac{d}{2}$, there is another time delay, t_{off}, before the switch S opens. (This delay is largely caused by the storage time of the transistor which is used as the switch S and is usually much longer than the delay T_{on}.) We can solve for t_c-t_b in equation 8 by noting that

$$I_{pp} = \frac{E_1 - E_2}{L}(t_d-t_b) \tag{9}$$

$$= \frac{E_1 - E_2}{L}(t_c-t_b + T_{off}) \tag{10}$$

therefore:

$$(t_c-t_b) = \frac{L}{E_1 - E_2}\,I_{pp} - T_{off} \tag{11}$$

Using this in equation 8,

$$d = -\frac{E_2}{L} T_{on} R_c + \frac{E_2}{2LC} T_{on}^2 - \frac{E_1 - E_2}{L} T_{off} R_c + \frac{E_1 - E_2}{2LC} T_{off}^2$$

$$+ I_{pp} R_c - \frac{I_{pp}}{2c} T_{on} - \frac{Ipp}{2c} T_{off} \qquad (12)$$

and solving this for the current amplitude in terms of the independent variables,

$$I_{pp} = \frac{\frac{d}{R_c} + \frac{E_2}{L} T_{on} \left(1 - \frac{Ton}{2R_c C}\right) + \frac{E_1 - E_2}{L} T_{off} \left(1 - \frac{t_{off}}{2R_c C}\right)}{1 - \frac{T_{on} + T_{off}}{2R_c C}} \qquad (13)$$

Equation 13 confirms the previous conclusion that if d is greater than zero, R_c must be greater than zero, or I_{pp} will grow very large. What is more, it shows that $2R_cC$ must be greater than $(T_{on} + T_{off})$ or a similar instability will result. These conditions are usually met in power regulators because the large electrolytic capacitors which must be used have fairly large R_cC products. It is not usually desirable, however, for R_cC to be very much larger than required for stability. As we shall see (para. B), a large R_cC requires a large LC in order to achieve a low level of ripple. Actually, R_c provides a phase lead in the feedback loop which compensates for the delays and hysteresis. If a capacitor with a very low R_cC were used, some other form of phase lead would have to be introduced to make the circuit stable.

Continuing toward an expression for the peak-to-peak ripple voltage, E_{pp}, note that we have already found the voltage (for switch S closed) in equation 7. Rearranging equation 7 and using equation 4,

$$e = -\frac{d}{2} - \left(\frac{I_{pp}}{2C} + \frac{E_2}{L} R_c\right) T_{on} + \frac{E_2}{2LC} T_{on}^2 - \left(\frac{I_{pp}}{2C} + \frac{E_1 - E_2}{L} R_c\right) (t-t_b) + \frac{E_1 - E_2}{2LC} (t-t_b)^2 \quad (14)$$

If $\frac{de}{dt} = 0$ at some time, t_{min}, while the switch is closed, e will reach its minimum at that time.

$$0 = \frac{de}{dt} = -\left(\frac{I_{pp}}{2c} + \frac{E_1 - E_2}{L} R_c\right) + \frac{E_1 - E_2}{LC} (t_{min} - t_b) \quad (15)$$

therefore:

$$(t_{min} - t_b) = \frac{I_{pp} L}{2(E_1 - E_2)} - R_c C$$

It is possible, however, for $\frac{de}{dt}$ to be greater than zero at all times between t_b and t_d (switch closed). Thus e is minimum at

$$(t_{min} - t_b)_m = \left[\frac{I_{ppL}}{2(E_1 - E_2)} - R_c C\right]_m = \begin{cases} \frac{I_{ppL}}{2(E_1 - E_2)} - R_c C \text{ if} > 0 \\ 0 \text{ if} \leq 0 \end{cases} \quad (17)$$

Noting that

$$\frac{I_{pp}}{2C} - \frac{E_1 - E_2}{L} R_c = \frac{E_1 - E_2}{LC} (t_{min} - t_b)_m \quad (18)$$

we may use equations 14 and 17 to obtain

$$e_{min} = -\frac{d}{2} - \left(\frac{I_{pp}}{2C} + \frac{E_2}{L} R_c\right) T_{on} + \frac{E_2}{2LC} T_{on}^2 - \frac{E_1 - E_2}{2LC} \left[\frac{I_{pp} L}{2(E_1 - E_2)} - R_c C\right]_m^2 \quad (19)$$

Note: $[\ ]_m$ = If this term becomes a negative value it is to be set equal to zero.

An exactly analogous equation applies for e_{max} -

$$e_{max} = \frac{d}{2} + \left(\frac{I_{pp}}{2C} + \frac{E_1 - E_2}{L} R_c\right) T_{off} - \frac{E_1 - E_2}{2LC} T_{off} + \frac{E_2}{2LC} \left[\frac{I_{pp}L}{2E_2} - R_cC \right]_m^2 \quad (20)$$

and by combining equations 19 and 20,

$$E_{pp} = e_{max} - e_{min}$$

$$E_{pp} = d + \frac{I_{pp}}{2C} (T_{on} + T_{off}) + \frac{E_2}{2LC} \left\{ 2R_cC\, T_{on} - T_{on}^2 + \left[\frac{I_{pp}L}{2E_2} - R_cC \right]_m^2 \right\} + \frac{E_1 - E_2}{2LC} \left\{ 2R_cC\, T_{off} - T_{off}^2 + \left[\frac{I_{pp}L}{2(E_1 - E_2)} - R_cC \right]_m^2 \right\} \quad (21)$$

where I_{pp} is given by equation 13.

B. Components

Equation 13 makes it clear that we must have

$$\frac{T_{on} + T_{off}}{2R_cC} < 1 \quad (22)$$

for stability. This presents no problem in practice because even the best electrolytic capacitors available are still fairly lossy. It seems likely, however, that a very lossy capacitor would be undesirable for other reasons. We can examine this question by relating the component parameters (including R_cC) to those conditions which would be specified by the application of the regulator. We can then insert values for the component parameters in these relations and observe how one parameter (such as R_cC) affects the requirements on any other parameter.

A good design is to adjust the input voltage range to have the worst ripple occurs at the highest input voltage (E_m)*. At this point the frequency is highest causing a low efficiency. Therefore, an efficient design must maintain the frequency below some practical maximum f_m at E_m. The time for one period is:

$$t = I_{pp} \frac{L}{E_1 - E_2} + I_{pp} \frac{L}{E_2}$$

$$= LI_{pp} \left(\frac{1}{E_1 - E_2} + \frac{1}{E_2}\right)$$

$$= \frac{1}{f}$$

To keep below f_m, a certain LI_{pp} product is required,

$$LI_{pp} \geq \frac{1}{f_m \left(\frac{1}{E_m - E_2} + \frac{1}{E_2}\right)} \tag{24}$$

Multiplying Eq. (13) by L gives,

$$LI_{pp} = \frac{\frac{LC}{R_c C} d + E_2 T_{on} \left(1 - \frac{T_{on}}{R_c C}\right) + (E_1 - E_2) T_{on} \left(1 - \frac{T_{off}}{R_c C}\right)}{1 - \frac{T_{on} + T_{off}}{R_c C}} \tag{25}$$

And solving for d,

$$d = \frac{R_c C}{LC} \left\{ LI_{pp} \left(1 - \frac{T_{on} + T_{off}}{R_c C}\right) + E_2 T_{on} \left(1 - \frac{T_{on}}{R_c C}\right) - (E_m - E_2) T_{off} \left(1 - \frac{T_{off}}{R_c C}\right) \right\} \tag{26}$$

*This is especially safe because ripple increases slowly with increasing input voltage at high inputs, but it increases rapidly with decreasing input voltage at low inputs. (See Figure 12, Section III.) However, efficiency requirements may dictate a worst case ripple at lowest input voltage.

where LI_{pp} is determined by Eq. (24)

Inserting this expression for d in Eq. (21) for the ripple and solving for LC gives.

$$LC = \frac{R_c C}{E_{pp}} \left\{ LI_{pp} \left(1 - \frac{T_{on} + T_{off}}{R_c C}\right) - E_2\, T_{on} \left(1 - \frac{T_{on}}{R_c C}\right) \right.$$

$$\left. - \left(E_m - E_2\right) T_{off} \left(1 - \frac{T_{off}}{R_c C}\right) \right\} + \frac{LI_{pp}}{2E_{pp}} T_{on} + T_{off}$$

$$+ \frac{E_2}{2E_{pp}} \left\{ 2\, R_c C \quad T_{on} - T_{on}^{\,2} + \left[\frac{LI_{pp}}{2E_2} - R_c C \right]_m^2 \right\}$$

$$+ \frac{E_m - E_2}{2E_{pp}} \left\{ 2R_c C \quad T_{off} - T_{off}^{\,2} + \left[\frac{LI_{pp}}{2E_m - E_2} \quad - R_c C \right]_m^2 \right\} \qquad (27)$$

This reduces to,

$$LC = \frac{1}{E_{pp}} \left[LI_{pp} \left[R_c C - \frac{T_{on} + T_{off}}{2} \right] \right.$$

$$+ \frac{E2}{2} \left\{ T_{on}^{\,2} + \left[\frac{LI_{pp}}{2E_2} - R_c C \right]_m^2 \right\}$$

$$\left. + \frac{E_m - E_2}{2} \left\{ T_{off}^{\,2} + \left[\frac{LI_{pp}}{2(E_m - E_2)} - R_c C \right]_m^2 \right\} \right] \qquad (28)$$

The required LC product and hysteresis d can then be calculated for given voltages, delay times, and capacitor quality using Eq's (24), (26), and (28).

This means, then, that to design for a given ripple E_{pp} at a given f (max) and a given E_1 (max), using a given transistor switching speed (T_{off}, T_{on}) and a given quality of capacitor ($R_c C$), requires a certain LC product which in turn determines the d required

(through equation 26) and the I_{pp} (through equation 25). This can be seen graphically in Figure 6 where the LC and d required to give a 5 mv E_{pp} are plotted as a function of R_cC. The values assumed for voltages and switching times are approximately as expected for the 12 VDC regulators. Figure 6 shows that for fairly lossy capacitors, the LC required is proportional to R_cC - and most of the weight of the regulator is concentrated in L and C. The capacitor should not be too good, however, because a smaller R_cC requires a smaller hysteresis. The hysteresis reaches zero at $2R_cC = T_{on} + T_{off}$, but for good noise immunity the hysteresis should be at least a millivolt.

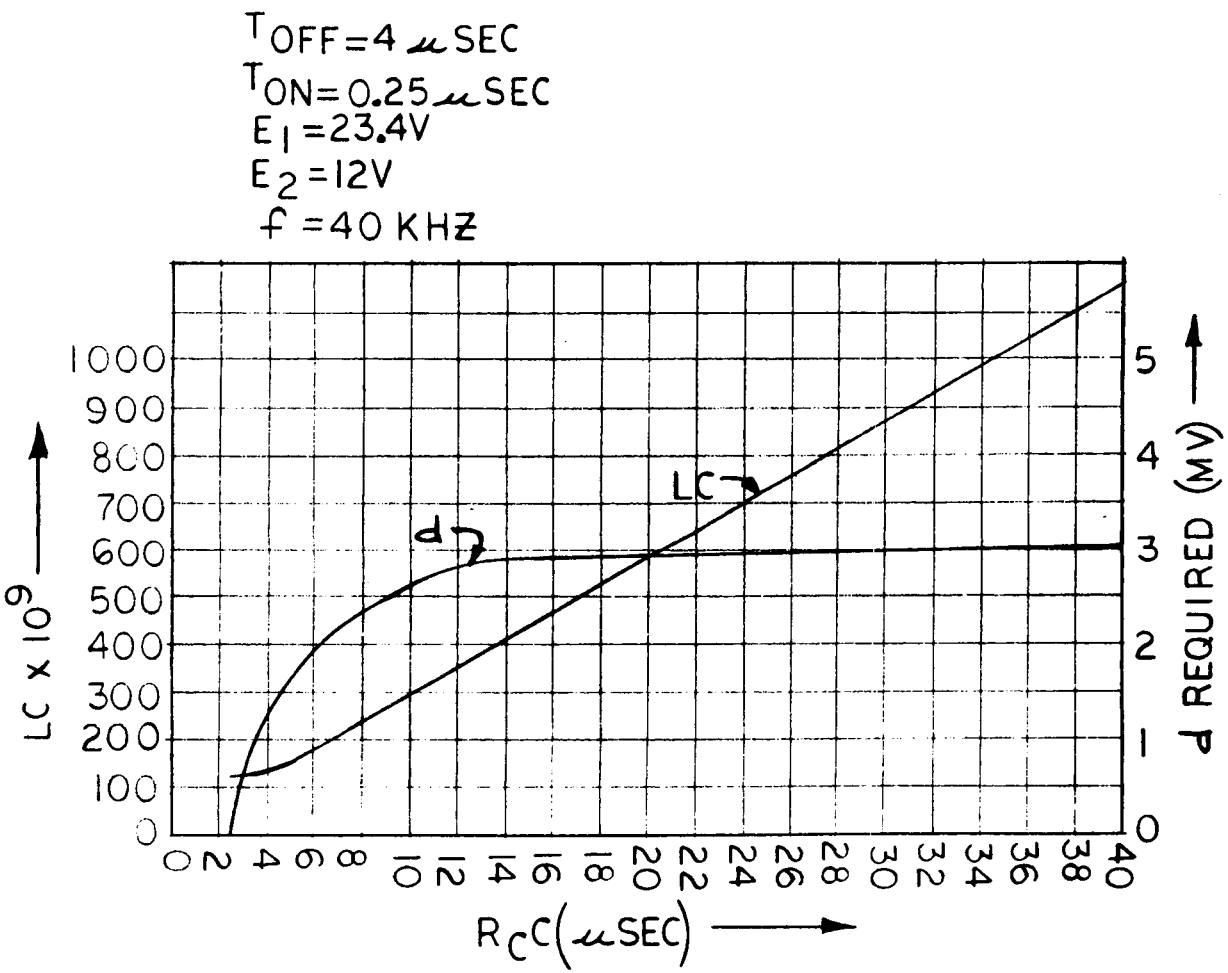


FIGURE 6. LC AND d REQUIRED FOR 5MV RIPPLE VS R_CC.